p-GaN Platform for Next-Generation GaN Complementary Transistors and Circuits

by

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ABSTRACT

Gallium nitride (GaN) integrated circuits (ICs) are receiving increasing attention because they offer compactness, reduced parasitics, and higher performance compared to discrete transistors or printed circuit board (PCB) integration. The p-GaN platform exhibits tremendous potential in power ICs and recently, in high temperature (500 °C) digital circuits. While the initial demonstrations offer promising results, several challenges remain. Notably, the lack of a monolithically integrated GaN complementary technology impedes the advancement of GaN power ICs.

This thesis aims to enhance the p-GaN platform (GaN-CMOS platform) (CMOS: complementary metal-oxide-semiconductor) through developing the next generation of GaN complementary technology (p-channel and n-channel field-effect transistors (FETs)). Based on the GaN-CMOS platform, the aggressive scaling of novel complementary transistors (self-aligned-gate p-FET and self-aligned metal/p-GaN-gate HEMT) is pursued. Alternative metallization schemes and a new technology for gate recess in GaN p-FETs are demonstrated. The unique characteristics of the p-FET are revealed through a combination of experimental measurements and TCAD simulations. The p-FET (based on GaN-CMOS platform) and p-GaN-gate n-FETs are analyzed for high temperature operation. Lastly, in order to aid the future design of more complex circuits based on the p-GaN platform, a device-to-circuit CAD framework was developed for GaN n-FET circuits and validated at high temperature up to 500 °C.

To the best of the author's knowledge, the above results represent the state-of-the-art in GaN complementary technology and GaN electronics based on the p-GaN platform. These findings are expected to deliver wider impact in the areas of power, RF/mixed-signal, and high temperature electronics.

Thesis supervisor: Tomás Palacios
Title: Clarence J. LeBel Professor of Electrical Engineering and Computer Science

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Chapter 1

Introduction

With the prevalence of electronics in our daily lives and its increasing role in our smart society, the demand for high performance, energy-efficient, compact electronics has seen an exponential increase. While traditionally microelectronics chips have been used for computation, there has been increasing needs for radio frequency (RF) and power electronics for emerging applications such as electric vehicles, 5G/6G telecommunication, and data centers. Among the various semiconductor technologies, gallium nitride (GaN) stands out as an excellent candidate for *both* RF and power applications, thanks to its wide band gap, high electron mobility, high breakdown field, thermal and chemical stability and more. Since the advent of the first AlGaN/GaN high electron mobility transistor (HEMT) (then called heterostructure field-effect transistor) in 1993, phenomenal advancement has been made the in the field of GaN electronics [1].

In the RF-GaN domain, GaN HEMTs are dominant in the RF power amplifiers in base stations (because only this technology is capable of delivering high power with high power-added efficiency (PAE) at microwave and mm-wave frequencies) [2,3]. Extensive research and development (R&D) efforts are under way to introduce GaN HEMTs for lower voltage applications in the RF front-end of cellular handsets, an application area traditionally dominated by Si LDMOS (laterally-diffused metal-oxide semiconductor) and GaAs pHEMTs (p: pseudomorphic).

In the power-GaN domain, GaN HEMTs promise fast switching with lower parasitics, therefore

greatly reducing the size of the passive components in the power converter [4, 5]. Therefore, GaN HEMTs have gained traction in fast charging power systems (e.g. for EV), as well as compact customer electronics (e.g. laptop/cell phone chargers). Furthermore, the rising performance of GaN power ICs (as opposed to discretely packaged power HEMTs) has offered compactness, and record levels of efficiency and power for data centers, power adapters, electric vehicles (EVs), and 5G telecommunication systems [2, 6, 7].

1.1 Motivation for GaN-CMOS and High Temperature Electronics

However, the lack of a GaN p-channel field effect transistor (p-FET) significantly increases static power dissipation (resulting from the use of n-type only enhancement-mode/depletion-mode logic) and prevents all-GaN integration (e.g. control loops, analog mixed-signal blocks) [8]. Power ICs face significant circuit design challenges because classic Si-CMOS gate driving techniques and circuits would not be feasible in all-GaN ICs [9]. On the other hand, the availability of high-side switching GaN p-FETs would improve the switching speed (avoiding the issue of limited common-mode transient immunity (CMTI) in the level shifter), therefore enabling more efficient and higher density power converters [10]. Therefore, the future introduction of GaN p-FETs would greatly benefit (1) mixed-signal integrated circuits, through suppression of static power dissipation [11]; (2) higher speed power converter ICs (e.g. for envelope tracking), by using the p-FET in high-side switching [10]; and (3) in higher linearity Class AB power amplifiers, through compensation of gate capacitance [12]. These applications would significantly improve the performance of GaN-based electronics.

Electronics operating at high temperature (HT), well above the effective 250–300 °C rating of silicon-on-insulator (SOI) technology, is another example of applications for which wide bandgap GaN is uniquely suited. These wide bandgap semiconductors are critical in extreme industrial applications (e.g. jet engines, nuclear reactors, deep oil well drilling), as well as in outer space, from

the solar system to exoplanetary exploration [13, 14]. Owing to inherent limitations of Silicon-on-Insulator (SOI) technology (thermal generation of carriers in conventional Si electronics), a promising solution is the use of GaN and other wide band gap materials. Thanks to their wide band gap, and superior electrical, mechanical, and chemical properties, these materials have enabled a wide range of devices. GaN electronics have demonstrated excellent performance in extreme environments (from cryogenic to high temperatures) across RF [15–17], power [18, 19] and mixed-signal applications [20]. Furthermore, much attention has also been paid to GaN-based circuits, mostly for high temperature, based on D-mode n-FETs, [21, 22] E/D-mode n-FETs, [23–25] and E-mode complementary (n+p) FETs. [26, 27] (D: depletion; E: enhancement; FET: field-effect transistor) In addition, GaN and III-N materials also offer a wider range of applications in power [28–30], RF [15, 17, 22], MEMS [31–33], memory [34], and solar cells [35]. Given the rapid advancement in GaN device technology for extreme environment applications, it is an opportune time to examine the high temperature performance of emerging GaN transistors such as p-FETs, as well as the harsh environment robustness of more established transistors like the p-GaN-gate HEMT, in order to further optimize these transistors.

1.1.1 Case Study of the RF Front End

Here, the case study of the RF front end, its existing issues and how a proposed GaN-CMOS technology could enable higher performance in the RF front end are discussed.

The realization of a high-data-rate uplink/downlink (peak rates of 10/20 Gbps) for 5G New Radio (NR) and beyond relies on the development of mm-wave transmitters, whose performance is in turn dominated by the linearity and power efficiency of the PAs [36]. Although GaN PAs have delivered unprecedented levels of power at K_a, W bands and beyond (e.g. 15 dBm at 205 GHz [37]), their limited linearity and the large PAPR in modern modulation schemes force GaN high electron mobility transistors (HEMTs) to operate at more than 6 dB power back-off, which significantly reduces the overall amplifier efficiency. New bottom-up approaches, based on innovations at the device-level, are highly desired to fundamentally improve linearity. Existing device-level tech-

niques focus on the engineering of the transconductance (g_m) in GaN HEMTs [38–41], but an area that has received little attention is the non-linear gate capacitance, which has been identified to result in significant AM/PM distortion in GaN PAs [42, 43].

The use of a p-FET to compensate the non-linear gate capacitance of RF transistors has been proposed for Si amplifiers [44]. However, the lack of a native p-type device prevents non-Si RF transistors from taking advantage of this technique. Using an existing Si PMOS device in combination with a GaN n-channel transistor leads to (1) complex heterogeneous integration, possibly 3D chip bonding [45], therefore higher parasitics; and (2) limited input voltage swings due to the breakdown voltage of Si PMOS, which will reduce maximum allowable P_{in} (hence P_{out}). Therefore, to retain the existing advantages of GaN HEMTs in PAs, a monolithically integrated GaN p-FET is necessary.

Envelope tracking (ET) has been widely used since 4G LTE to improve the efficiency of PAs and the battery lifetime of cellular handsets [46,47]. In 5G FR2, for a conservative uplink/downlink rate of 1/5 Gbps, even with a high-order modulation scheme like 64-QAM, the bandwidth needs to be $\sim$ 800 MHz [48]. This implies that the switching speed of the DC-DC converter in the ET needs to be $\sim$ 1.5 GHz (2 $\sim$ 3$\times$ bandwidth). To worsen the situation, in a typical high efficiency hybrid ET, the DC-DC converter already constitutes the bottleneck in the bandwidth [49]. The use of existing GaN n-FETs in the high side switching of the power converter requires a level shifter which results in a degradation of the bandwidth. Alternatively, Si p-FETs may be used, but at the expense of lower voltage rating and higher switching. Therefore, the development of a high performance wide band gap p-channel high-side switch, such as a GaN p-FET, is required to widen the bandwidth of ETs.

GaN-CMOS technology, if successful, would be a fundamental device-level advancement that could bring about advancements in the RF front end. A simplified schematic of the RF transmitter, consisting of the power amplifier, is illustrated in Fig. 1.1(a). Specifically, two areas are discussed:

1. GaN CMOS DC-DC converter for use in hybrid ET: The use of a GaN p-FET switch is proposed for a wide bandwidth dynamic power supply to be used in 5G PAs (Fig. 1.1(a)). In the

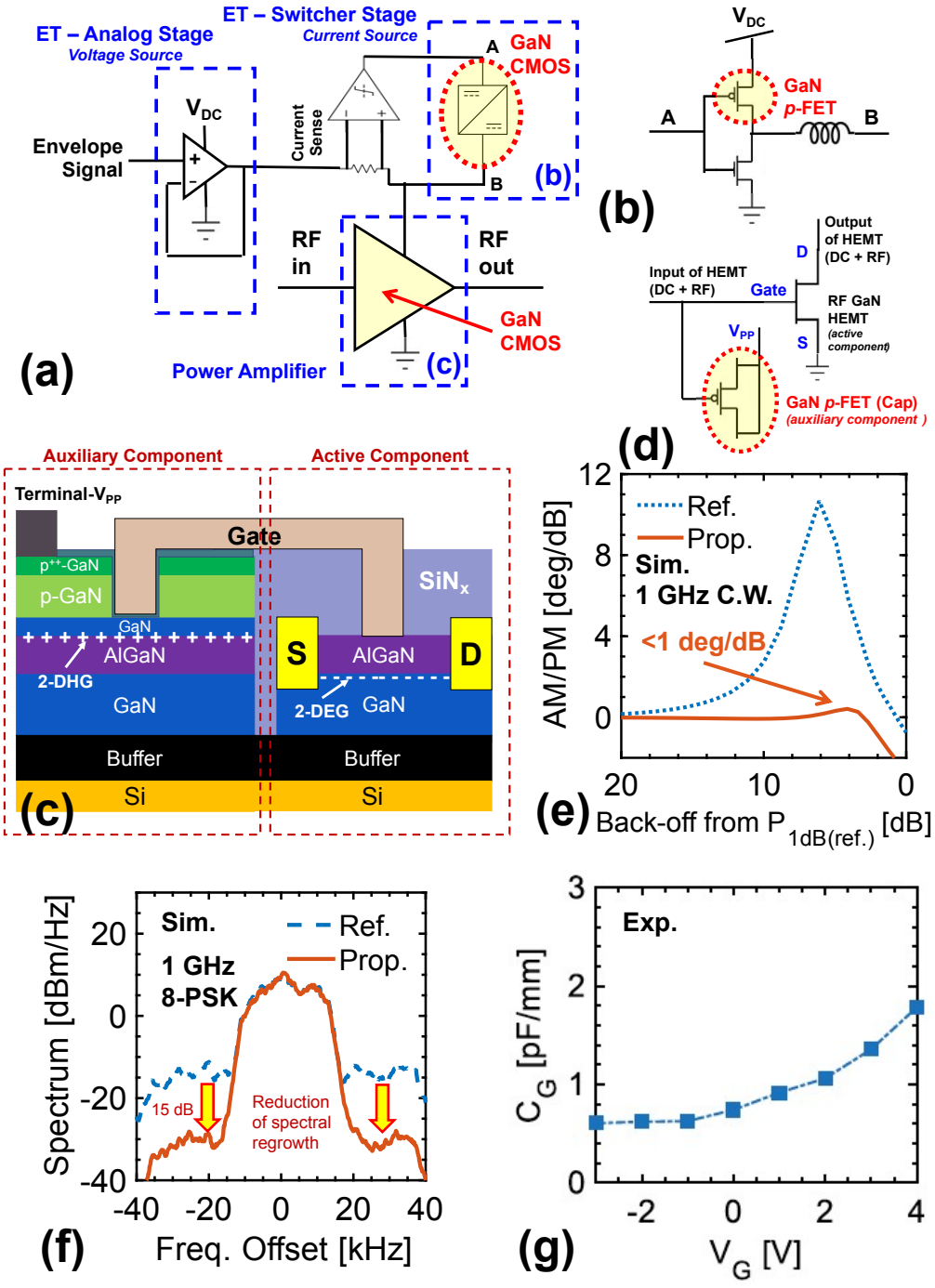


Figure 1.1: Applications of GaN-CMOS technology in the RF front end. (a) Schematic of the RF transmitter. The proposed novel components based on GaN-CMOS technology are highlighted. (b) Circuit diagram of the proposed DC-DC converter used in the switcher stage of the ET. (c) Proposed integrated GaN-CMOS device to achieve higher linearity. (d) Simplified circuit model of the proposed linearized device used in the simulations. Proof-of-concept simulations indicate promising performance: (e) One-tone load-pull at 1 GHz, showing significant reduction in AM/PM to < 1.5 deg/dB. (f) 1 GHz 8-PSK operation, showing reduction in spectral regrowth. Significant improvement in EVM (by > 60 %) at higher receiving channel powers was observed. (g) Preliminary experimental results of a linearized capacitance profile of a GaN n-FET with $V_{th} = 2$ V and ON-OFF ratio of 10^8.

switcher stage (Fig. 1.1(b)), the GaN p-FET would be gated by pulses from the analog stage. Here, no level shifters are required because the high-side switching is performed by the p-FET. Therefore, assuming p-FETs with high switching performance are deployed, GaN-CMOS technology is expected to realize wide bandwidth envelope trackers in the power management ICs.

2. Linear GaN amplifier using "capacitance compensation": An integrated device which could offer higher linearity has been designed based on the GaN CMOS platform (Fig. 1.1(c)). Extensive proof-of-concept simulations (Fig. 1.1(d)) reveal that, the linearized device yields significant improvement in linearity (Fig. 1.1(e)–(f)) [12]. In addition, preliminary experimental results reveal linearized gate capacitance for a RF n-FET (Fig. 1.1(g)), attesting to the feasibility of the proposed concept. While existing demonstrations of the proposed GaN CMOS platform have been on GaN-on-Si wafers, the technology could be easily transferred to GaN-on-SiC wafers to provide optimal environment for maximum microwave power performance.

1.2 Early Work on GaN-CMOS

As a disclaimer, here (and throughout the thesis), the term "GaN-CMOS" refers to the concept of complementary GaN-based transistors (GaN-based p-FET and GaN-based n-FET), similar to the Si-CMOS technology (Si-PMOS and Si-NMOS FETs) prevalent today. The concept may be further extended to complementary transistors based on other III-N materials. In the case of specific transistor structures, the term "complementary transistors" or "complementary technology" (CT) will be used instead, because "CMOS" contains references to the MOS (metal-oxide-semiconductor) structure. "GaN-CMOS" does not typically require a carrier inversion layer as is the case in more conventional Si-CMOS. In this thesis, unless otherwise stated, "complementary transistors" does not refer to the novel device architecture "complementary transistor (CFET)" proposed for Si advanced logic nodes, though GaN-CFET would be a promising area for future

work [50].

Pioneering experiments have been conducted in the area of GaN-CMOS. Most experiments have focused on demonstrating p-FETs (which is the missing piece of the puzzle in a GaN-CMOS technology), while some significant works of GaN-CMOS by Chu, Hahn, Nakajima, Chowdhury, Zheng *et al.* [11,26,27,51,52] have demonstrated integrated GaN complementary transistors and/or circuits. In recent years, this rapidly advancing field has witnessed the demonstrations of: (1) complex complementary circuits [53]; (2) high performance p-FETs using (i) various epitaxial structures [54–57, 57–59], (ii) novel transistor architectures (e.g. FinFET [58, 60–63]), and (iii) process technologies [53, 64–67]. Thus far, discrete III-N p-FETs have received significant attention, but equal attention should be paid to their monolithic integration with n-FETs.

Broadly speaking, there are two categories of GaN-CMOS platforms. First is the epitaxial regrowth approach, where the n-channel and p-channel are formed separately. In the experiment of Chu *et al.* (2016), the as-grown epitaxy consists of AlGaN (for n-channel). Then, after some fabrication steps, the p-GaN is regrown and patterned in selective regions (where the p-FET will be located). The second category, which is more prevalent in the literature, is the co-existence of n-channel and p-channel on the same epitaxy, typically by as-grown p-GaN/AlGaN/GaN (or variant). There are advantages and disadvantages of each approach. The first approach allows for independent optimization of the n-channel and p-channel separately, but regrowth of p-GaN is costly, and requires careful processing. Much optimization would be required to ensure high quality of the regrown p-GaN (and the interface with AlGaN), compared to conventional as-grown p-GaN (*in-situ* with AlGaN/GaN). The second approach allows for the easy integration of n-FET and p-FET, by designing transistor structures which make use of each channel. The challenge is that the properties of the n-channel and p-channel (therefore, n-FET and p-FET) are inevitably coupled because both channels rely on the *same* AlGaN layer as the polarization-inducing layer. Therefore, for such structures, the challenge in integration is more than just the fabrication. At this stage, basic integration of n-FET and p-FET has been demonstrated in several early works cited above. Two major challenges need to be addressed for such integrated GaN-CMOS platforms: (1)

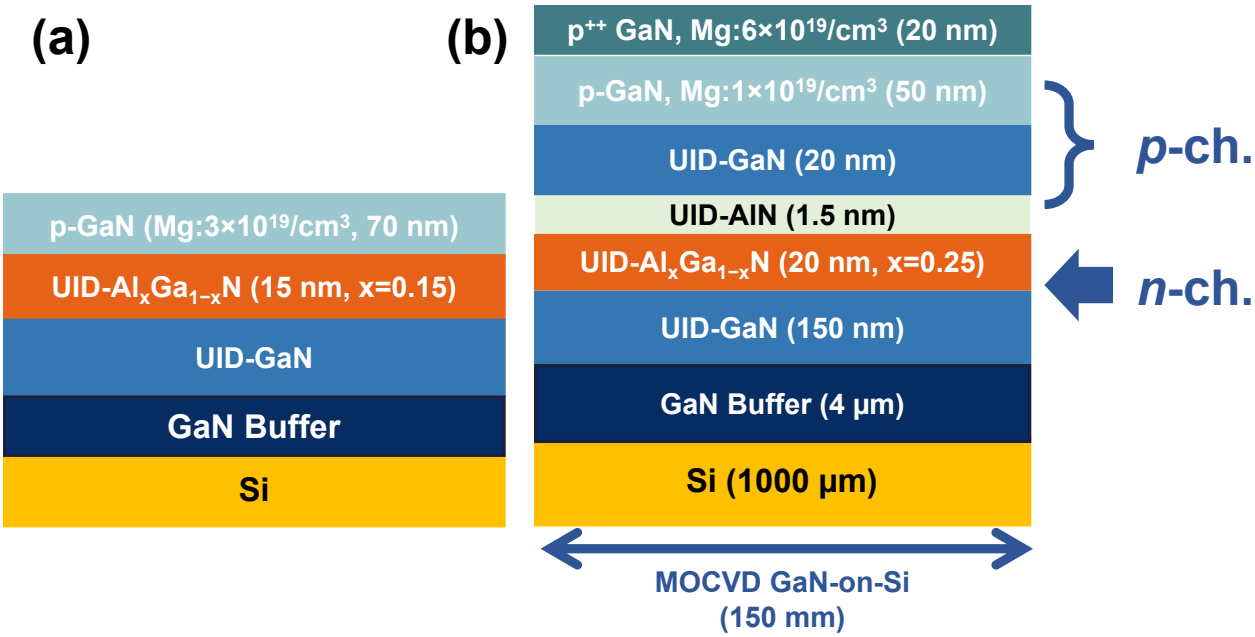


Figure 1.2: GaN-CMOS platform. (a) A conventional epitaxy for p-GaN-gate power HEMT, for illustrative purpose. (b) Epitaxial structure of the GaN-CMOS platform used in this thesis. Note that all doping levels are nominal values provided by the supplier. Actual doping profile is affected by non-idealities such as the Mg doping delay and memory effect.

how to ensure high performance transistors in *both* n-FET and p-FET, (2) how epitaxial features introduced for one type of transistor would affect the performance of the other type of transistor. These challenges will be taken into full consideration in this thesis.

1.3 GaN-CMOS Platform Used in This Thesis

Before introducing the GaN-CMOS platform, it is insightful to review the conventional p-GaN platform, typically used for power HEMTs. A typical epitaxy is shown in Fig. 1.2(a). At the top of the conventional AlGaN/GaN epitaxy (used for E-mode HEMTs), a p-GaN layer is added to ensure normally-off operation, by depleting the 2DEG channel (AlGaN/GaN interface) at zero bias conditions.

The GaN-CMOS platform used in this work is inspired by the conventional p-GaN platform, but contains several notable differences. As presented in Fig. 1.2, the GaN-CMOS platform consists of p^{++}-GaN, p-GaN, GaN, AlN, AlGaN and GaN layers (unintentionally doped (UID) if

doping is not specified). The p^{++} layer (with a high doping level of 6×10^{19} cm^{-3}) would benefit the formation of ohmic contacts to p-GaN. Another feature is the insertion of UID-GaN, which seeks to reduce carrier scattering in the GaN/AlGaN interface (due to significantly less doping). It could be thought of as a "spatial separation" of the dopant from the quantum well, which is a feature that gives the high mobility of electrons in GaAs pHEMTs.

The GaN-CMOS platform features the co-existence of the p-channel and n-channel. The p-channel consists of the p-GaN (bulk channel) and the 2DHG channel at the GaN/AlGaN interface, a property of this epitaxy which will have profound implications in the p-FET characteristics (refer to Chapter 4). The n-channel is formed by the AlGaN/GaN 2DEG, which is depleted at zero bias. While the epitaxy could be grown in a variety of substrates (e.g. SiC, sapphire, Si, AlN), in this work, the Si (111) substrate is used due to the scalability (large diameter wafers, a desired property of GaN-CMOS technology, refer to Chapter 1.4) and low cost. For similar reasons, MOCVD is used (instead of MBE), despite several advantages of MBE (e.g., maximum p-GaN doping could be higher in MBE [68]).

1.4 Requirements of Next-Generation GaN-CMOS Technology

While early experiments have indicated the feasibility of GaN-CMOS, further advancements in several aspects of this technology are needed to realize the proposed circuit-level applications. In fact, based on the GaN-CMOS platform of this work (Fig. 1.2(b), less AlN layer), significant progress has been made in the performance of p-FETs [61, 65, 69, 70]. Therefore, the question is, how could we push GaN-CMOS technology further to make it a reality?

At this stage of GaN-CMOS research, this thesis advocates an application-driven perspective to the issue of advancing GaN-CMOS platform. Fig. 1.3 lists various requirements (of the GaN-CMOS technology as a whole) and the proposed solutions adopted in this thesis.

1. Easy integration of n-FET and p-FET. As mentioned earlier in this chapter, a major advantage of the p-GaN/AlGaN/GaN epitaxy (or variants) is the co-existence of both n-channel

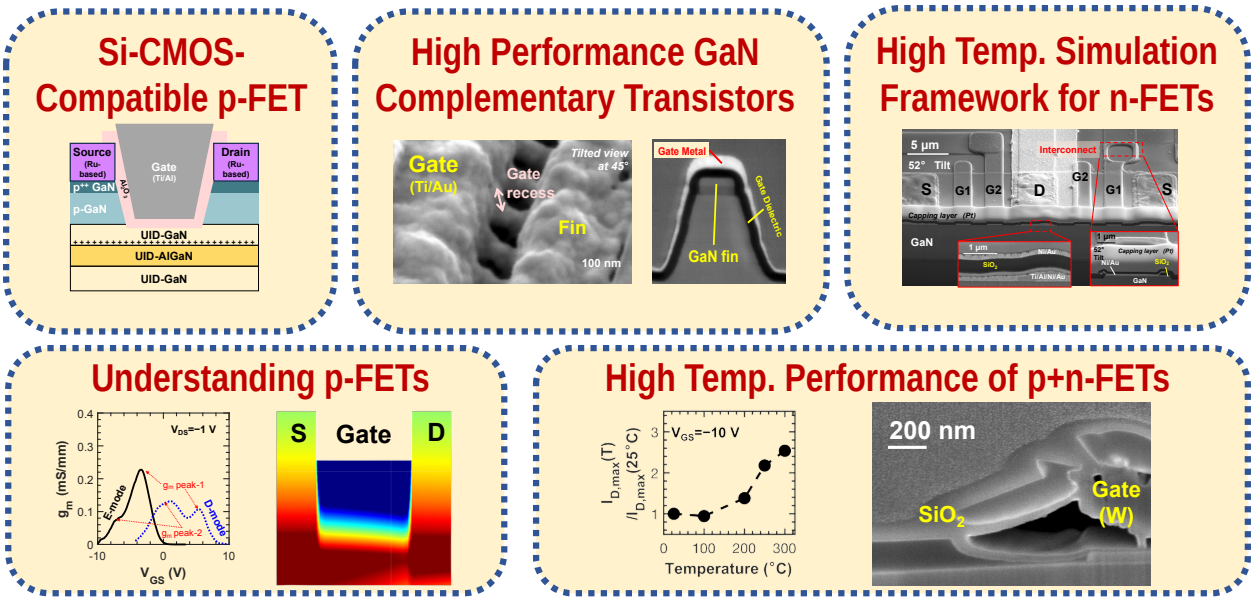


Figure 1.3: Advancing next-generation GaN-CMOS technology through an application-driven perspective. The requirements of the technology and the proposed solutions (adopted in this thesis) are indicated.

and p-channel on the same epitaxial structure. This serves as the basis for the easy integration. This avoids the need for costly regrowth steps. In earlier work, a regrowth-free GaN complementary circuit (logic inverter) was demonstrated, therefore proving the feasibility of the GaN-CMOS platform for easy integration [26]. Later, experiments of similar integration on similar epitaxial structures have been reported by other researchers (Chapter 1.2), therefore attesting that the integration results are reproducible. This thesis builds upon this capability where n-FETs and p-FETs are monolithically integrated.

2. Scalability of the wafer platform. MOCVD GaN-on-Si were epitaxially grown by commercial suppliers on 150 mm and 200 mm Si (111) wafers. The use of larger diameter wafers is in line with industry trends (e.g. 300 mm reported by Intel Corp. [45]) and also benefits from the sophistication of processing equipment (designed for larger diameter wafers). Scalability and MOCVD growth (significantly higher throughput than MBE) are major considerations for the commercialization of GaN electronics; the vast majority of the commercially available GaN electronics are grown by MOCVD.

3. High performance p-FET and n-FET. The need for high performance transistors is a central requirement of any technology, especially in GaN-CMOS which is an emerging concept. Furthermore, considering Requirement 1, it was decided from the start that such high performance complementary transistors need to be based on the same GaN-CMOS platform, so as to attract IC designers to adopt the technology. The high performance p-FETs are only as impactful as they can be, *if and only if* they can be properly integrated with n-FETs for IC applications. In this thesis, the approaches to achieving higher performance are device innovation and process optimization. Emphasis is placed on the demonstrations of *novel* (as opposed to solely optimized) device features and process (e.g., self-alignment in p-FET and n-FET gate).

4. Si-CMOS-compatible metallization. In the early demonstrations of GaN HEMTs and p-FETs, a gold-based process was used, which precludes them from being fabricated in Si-CMOS-compatible foundries. Si-CMOS-compatibility is mutually beneficial for both GaN-CMOS technology and the foundries – on one hand, such a technology would be more readily uptaken by the foundries, therefore increasing the impact of the GaN-CMOS technology; on the other hand, GaN-CMOS technology could benefit from the sophisticated process capability in Si foundries to greatly improve on the process stability and quality for GaN-CMOS technology. This work explores the use of Ru-based S/D contacts, and demonstrates their integration in p-FETs.

5. High temperature operation. The characterization of complementary transistors under HT stress is desired to ensure: (1) HT operation for a variety of industrial applications (e.g. automotive), (2) reliable operation at high power, (3) reduced cooling and thermal management needs, and (4) harsh environment electronics (e.g. for hypersonic aircraft and outer space exploration). While there are some early characterization of GaN p-FETs at HT, with the rapid advancements in the field, it is important to characterize the latest p-FETs. Furthermore, the p-FETs based on the GaN-CMOS platform (addition of UID-GaN) shows a distinct behavior

at HT, as compared to p-FETs based on a conventional p-GaN/AlGaN/GaN platform. For n-FETs, given that their temperature-dependent characteristics are well studied, the characterization under realistic extreme environment conditions is the natural next step.

Requirements 1–2 have been addressed in early works, in which the author has made substantial contributions. Considering the above, this thesis focuses on innovative solutions for requirements 3–5. In this way, this thesis aims to make fundamental contributions to the vision of next-generation GaN-CMOS technology and its adoption.

1.5 Objectives and Methodology

The objectives and methodology of the thesis are as follows:

1. To advance GaN complementary transistor technology through exploring the scaling limits of such transistors.

2. To explore the potential of the proposed GaN complementary transistors (especially p-FET) for commercialization, through Si-CMOS-compatible metallization.

3. To understand the unique transistor characteristics of p-FETs through a combination of measurements and TCAD simulation/modeling.

4. To develop a device-to-circuit level simulation framework to aid the scaling-up of transistor/basic circuits on the p-GaN platform.

5. To study the high temperature performance of GaN complementary transistors, and the harsh environment robustness/degradation of p-GaN-gate HEMTs (n-FETs).

1.6 Organization of the Thesis

This thesis, with the central theme of advancing GaN complementary transistors and circuits based on a p-GaN platform, is organized as follows.

Chapter 2 "Highly Scaled GaN Complementary Technology" presents the pursuit of high performance in complementary GaN transistors (p-FET and n-FET) based on the GaN-CMOS platform. Through aggressive scaling in the channel length and fin width dimensions, and the use of self-aligned features, highly scaled p-FETs (self-aligned-gate p-FETs) and n-FETs (self-aligned W/p-GaN gate HEMT) with record performance are demonstrated. The trends of scaling are studied. An improved ICP-RIE p-GaN/AlGaN selective etch is developed.

Chapter 3 "Si-CMOS-Compatible GaN p-FET" addresses another major roadblock towards the commercialization of GaN-CMOS technology, which is the (lack of) Si-CMOS-compatible metallization. A Ru-based S/D-contact technology was developed and optimized. Ru-based S/D contacts are integrated into a self-aligned p-FET (ohmic-first) process. A novel gate recess technology was developed for E-mode p-FETs.

Chapter 4 "Unique Design Space of GaN p-FETs" seeks to deepen the understanding of the state-of-the-art p-FETs based on the GaN-CMOS platform. The impact of gate recess on the transfer characteristics of the p-FET is analyzed through TCAD simulation, which was later verified by experiment. TCAD simulation indicates the existence of the two components of the channel, and their contributions to the transistor characteristics. Furthermore, the impact of a realistic p-doping profile (as opposed the idealized uniform doping) is studied and reveals trade-offs in the p-FET characteristics.

Chapter 5 "p-FETs and n-FETs for High Temperature Operation" examines the HT performance of the p-FET and n-FET. A novel p-FET (with Ru-based S/D, described in Chapter 3) was measured at HT up to 300 °C. The DC characteristics are analyzed. Newly developed understanding from Chapter 4 is used to explain the unique HT behavior of the p-FET. The characterizations of n-FET (p-GaN-gate HEMT) at HT and after harsh environment exposure are briefly discussed. The concept of a p-channel junction FET (JFET) is proposed to achieve HT robust p-FETs, and preliminary process development is conducted for the short-channel p-n junction gate.

Chapter 6 "Towards DTCO in high temperature GaN-on-Si technology: a CAD framework up to 500 °C" presents a device-to-circuit simulation framework for novel GaN electronics, using the

case study of n-FET-based GaN HT electronics. Through detailed characterization of the transistors and circuits at HT up to 500 °C, models are established and verified at the circuit-level. This work serves as a stepping stone for the eventual DTCO of GaN n-FET-based HT electronics, and also a future simulation framework for GaN-CMOS technology.

Chapter 7 "Conclusion and Future Work" summarizes the work and proposes several areas of future work, ranging from the device (transistor)-level, to circuit-level (proof-of-concept circuit demonstrations of GaN-CMOS), and the need for a robust simulation framework.

Chapter 2

Highly Scaled GaN Complementary Technology

The materials in this chapter are partially based on the following publications. The published materials in the publications mentioned below are reused with permission.

Q. Xie *et al.*, "Highly-Scaled Self-Aligned GaN Complementary Technology on a GaN-on-Si Platform," *2022 International Electron Devices Meeting*, pp. 35.3.1–35.3.4, Dec. 2022. © 2022 IEEE [71]

Q. Xie *et al.*, "Highly Scaled GaN Complementary Technology on a Silicon Substrate," *IEEE Transactions on Electron Devices*, vol. 70, no. 4, pp. 2121–2128, Apr. 2023. [72]

2.1 Introduction

As discussed in Chapter 1.2, several recent works have studied the feasibility of a GaN complementary technology (CT). In view of the above application requirements and among the various options, the GaN CT platform in [26] based on p-GaN/UID-GaN/AlGaN/GaN heterostructure stands out as a promising candidate. This work seeks to advance the performance of GaN p-FET and

n-FETs on this platform, through a combination of device innovation and process optimization. A distinctive feature of these transistors is the aggressive scaling in the p-FET and n-FET, including self-aligned (SA) gate etch. It is noted that, aggressive scaling has been adopted in a wide range of novel transistors to improve their performance [17, 73], and will be a key strategy pursued in this work.

The organization of this chapter is as follows. The concepts of the p-FET and n-FET are explained in Chapter 2.2. The fabrication and characterization of the p-FET are presented in Chapter 2.3, followed by the same aspects of the n-FET in Chapter 2.4. Chapter 2.5 presents a benchmarking of the proposed GaN CT and an overview of the areas of future research, followed by Chapter 2.7 which concludes the article.

2.2 Epitaxial Platform and Transistor Architectures of GaN CT

The starting material is the GaN-CMOS platform as shown in Fig. 1.2(b). The epitaxial structure ("Epi-1", Fig. 2.1(a)) is modified from earlier work [26] by inserting a 1.5 nm AlN (in actual implementation, high Al composition AlGaN) layer. The use of an AlN layer allows for polarization enhancement of the p-channel charge density [55] and a better etch stop during the selective etch of p-GaN/UID-GaN over AlGaN (a key process step for the n-FET). Both p-FETs and n-FETs were fabricated on this structure (Fig. 2.1(b)–(d)). The same epitaxial structure of Fig. 2.1(a) was processed to realize the p-FET and n-FET (Fig. 2.1(b)). In this chapter, unless otherwise stated, the p-FET and n-FET refers to GaN-based transistors.

The transistor architecture of the p-FET is the FinFET which features self-alignment between the ohmic and gate. A representative p-FET is shown in Fig. 2.1(c). Channel length scaling of p-FETs is critical to overcome the low hole mobility in these transistors (experimentally measured to be typically $< 30\ \mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$) and to take advantage of field-induced acceptor ionization [69, 70]. To this end, a SA FinFET architecture [61] was adopted in this work as it offers new opportunities for

p-FET design. The impact of fin width scaling and recess depth on these transistors was studied. Further improvement in transistor performance was also contributed by optimizations to the key process steps of the proposed p-FET, which will be described in Section 2.3.1.

This work also seeks to improve the performance of GaN n-FETs based on the GaN CT platform through the development of a gate technology where the gate metal is self-aligned (SA) to the p-GaN region. The realization of E-mode n-FETs is highly desired for a wide variety of applications, including power electronics, as well as digital and RF integrated circuits (ICs), where the bias circuitry could be simplified by eliminating the need of a third bias terminal (V_{SS}) [74]. Recent efforts have also explored the potential of such short-channel p-GaN-gate HEMTs for RF applications, including in PA and LNA [75, 76].

Approaches to the realization of GaN E-mode n-FETs include, F-plasma treatment of gate region [77], MIS-recessed gate [78], FinFET/tri-gate [79] and p-GaN-gate [26]. In this work, the p-GaN-gate n-FET is chosen because (1) easy integration with p-FET (Fig. 2.1(b)) and other power IC components [8]; (2) minimum degradation of as-grown gate surface (i.e. no photoresist or etching), which reduces hysteresis and trapping issues; (3) demonstrated performance and robustness in GaN circuits at high temperature (up to 500 °C) [80, 81].

While numerous p-GaN-gate HEMTs have been reported in the literature, the introduction of self-alignment between the metal electrode and the p-GaN would be beneficial for: (1) achieving a shorter p-GaN gate length, because the alignment tolerances needed for the metallization would not be applicable; (2) reduction of gate capacitance, which is key for high-speed low/medium-voltage power ICs and analog mixed-signal applications.

The planar architecture was chosen for the n-FET (p-GaN-gate HEMTs). A representative p-FET is shown in Fig. 2.1(d). The choice of the planar architecture is not just due to process simplicity, but also due to other considerations. Most conventional power HEMTs rely on the planar architecture and excellent performance has been obtained. Furthermore, looking at GaN-CMOS holistically, the key performance improvement needs to originate from the p-FET (with respect to the n-FET). The key for n-FET is to ensure that competitive performance is maintained.

(As will be shown in Chapter 2.5, the n-FET of this work also achieves competitive performance.) Having said that, there are demonstrations of E-mode FinFETs (tri-gate) based on the p-GaN-gate structure [82]. If the FinFET (tri-gate) concept were to be adopted for the E-mode n-FET, the range of device designs would not just be limited to p-GaN-gate FinFETs, but also junction tri-gate FETs using NiO and LiNiO [83, 84].

2.3 GaN p-FET

2.3.1 Self-Aligned GaN p-FinFET Process Flow

The process flow of the p-FET is an optimized version of the baseline flow as reported in [61], and is illustrated in Fig. 2.2. Here, the entire flow is described in detail, with the key improvements highlighted to showcase the novelty of this work. The flow begins with the S/D metallization using Ni/Au/Ni (30/50/30 nm) deposited by electron beam evaporation and patterned by a lift-off technique. Then, the S/D metal is alloyed at 550 °C for 45 min. in N_2/O_2 (1 : 1 ratio). The annealing of Ni/Au in O_2 allows for the formation of Ga vacancies in the p-GaN (through Ga-Au alloy), and the formation of NiO_x which has high workfunction to p-GaN [85, 86].

Next, the fin lithography is performed using 4% hydrogen silsesquioxane (HSQ), which results in a $\sim$ 70 nm layer of HSQ. A fin width of 20 nm is achieved here. Next, the fins are patterned through etching by BCl_3/SF_6 plasma and SiO_2 (formerly HSQ) as mask. Note that the fins extend from the source to the drain. The fins were aligned to the *m*-plane, in order to ensure smooth sidewalls as discussed later [87]. The SiO_2 (formerly HSQ) on the fins is removed using a quick ($\sim$ 2 min.) buffered oxide etch (BOE 7 : 1) dip. Then, a SA gate recess (SA to the S/D) is conducted using the same Cl_2/BCl_3 plasma RIE recipe as above. A time-controlled etch is used. A medium-power BCl_3/SF_6-RIE (etch rate of $\sim$ 1 nm/min.) was used for these steps as a compromise among damage to ohmic contact, fin etch-induced damage, and good etch geometric profile. The optimized process was capable of achieving fin widths of 20 nm at L_{SD} of $<$ 200 nm. The SA architecture ensures that the access region (and access resistance) is negligible and that the entire

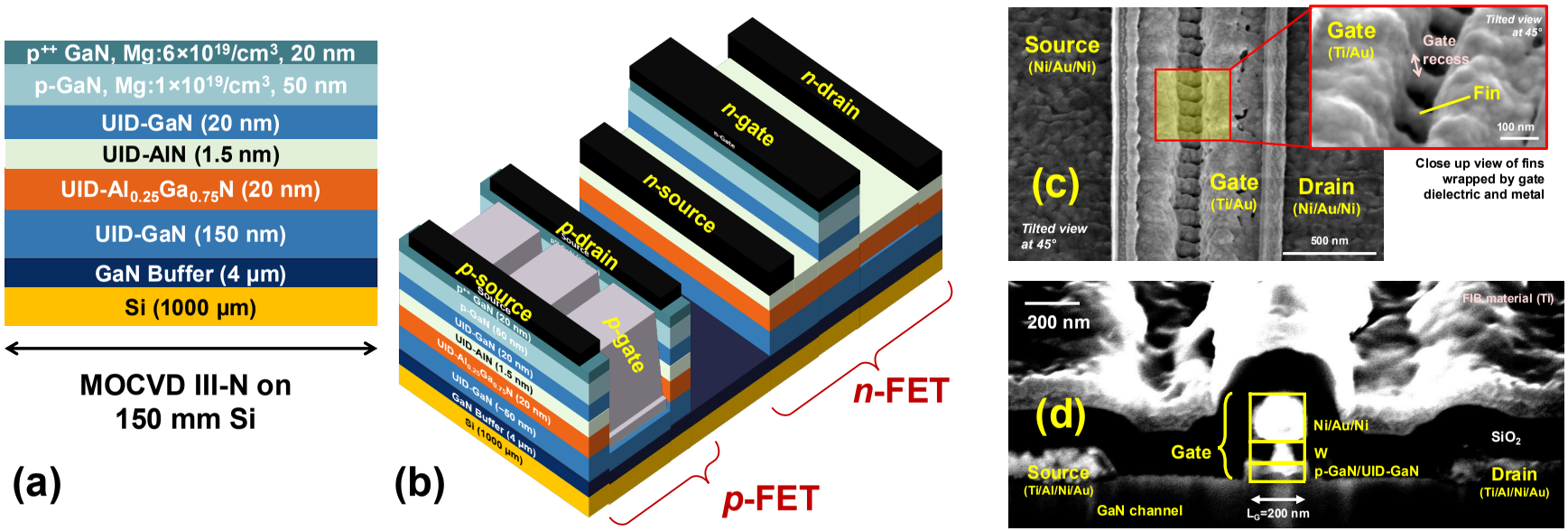


Figure 2.1: Highly-scaled GaN complementary technology (CT). (a) Epitaxial structure. (b) Device structures of p-FET (SA FinFET) and n-FET (SA-gate p-GaN-gate HEMT) based on the same GaN-on-Si platform as illustrated in Fig. 2.1(a). (c), (d) Scanning electron microscopy (SEM) images of representative p-FET and n-FET, respectively.

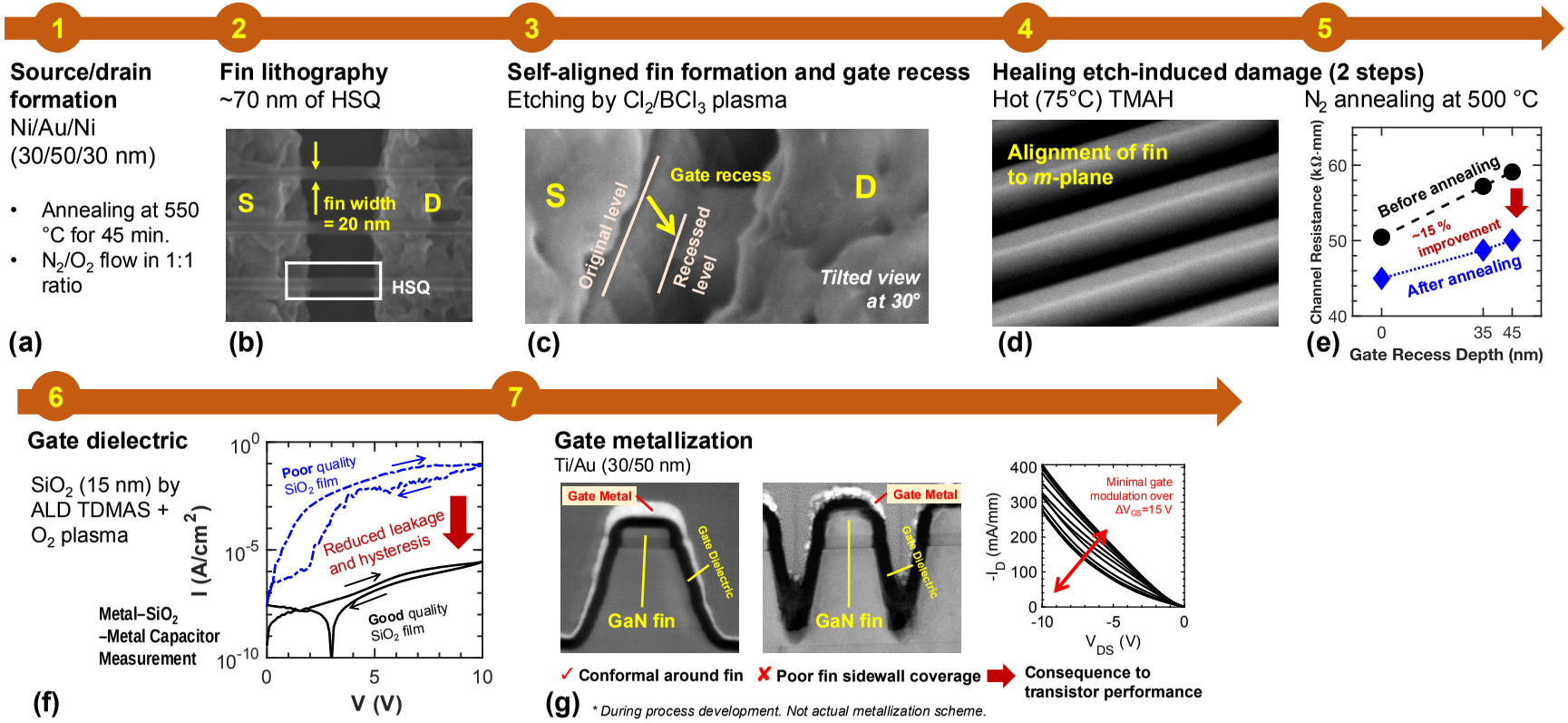


Figure 2.2: Process flow of the self-aligned (SA) FinFET: (a) source/drain (S/D) formation using Ni/Au/Ni. (b) Fin lithography. An improved fin lithography process using thinner HSQ (70 nm) has allowed for aggressive scaling of the fins down to 20 nm fin width. The HSQ thickness was carefully calibrated to achieve a balance between fine lithography and subsequent etch resistance. Fins were aligned to the m-plane. (c) SA gate region. Two etches were conducted using medium-power Cl_2/BCl_3 plasma, (1) fin etch, using SiO_2 (formerly HSQ) as mask, which ensures self-alignment to S/D contacts, (2) after removal of SiO_2, SA gate recess using S/D contacts as mask. (d) Healing etch-induced damage (step 1), tetramethylammonium hydroxide (TMAH) treatment at 75 °C for 5 min. (e) Healing etch-induced damage (step 2), N_2 annealing at 500 °C for 1 h. $\sim$ 15 % improvement in the channel resistance for various recess depths is observed. (f) Atomic layer deposition (ALD) of gate dielectric (SiO_2). Typical characteristics of metal-insulator-metal (MIM) capacitors (with variation in quality of SiO_2 films) is presented. (g) Gate metallization. Conformal gate metallization is extremely important for gate control, especially for closely packed fins.

length of the fin ($= L_{SD}$) is gated. Otherwise, an access region with the fin architecture would greatly increase the access resistance (normalized by total width, taking fin pitch into account), and would nullify the positive impact of channel length scaling in these p-FinFETs.

When compared to a planar channel, the fin channel has more surface area exposed to RIE plasma. Therefore, several steps were conducted to heal etch damage. Two steps are used to heal the etching damage, namely the tetramethylammonium hydroxide (TMAH) treatment at 75 °C for 5 min., which ensures the smoothness of the m-plane sidewalls, and N_2 annealing at 500 °C for 1 h. ~ 15 % improvement in the channel resistance for various recess depths is observed. Then, atomic layer deposition (ALD) of gate dielectric (SiO_2) is conducted using tris(dimethylamino)silane (TDMAS) precursor and O_2 plasma at 250 °C. Typical characteristics of metal-insulator-metal (MIM) capacitors (with variation in quality of SiO_2 films) is presented. For a representative MIM capacitor fabricated with a good quality film, low hysteresis (< 1 V) and leakage (< 1 $\mu A/cm^2$) (at 5 V) could be obtained. To the contrary, for a representative MIM capacitors fabricated with a poor quality film, high leakage ~ 10 mA/cm^2) is observed, together with highly fluctuating I-V measurement. In the worst case, such films are permanently degraded after a few repeated measurements. The gate dielectric quality and p-GaN/dielectric interface make a significant contribution to the device switching characteristics, therefore making this an area of active research [88, 89].

The last step is the gate metallization, which is done by a sputtering and lift-off process. Conformal gate metallization is extremely important for gate control, especially for closely packed fins. Through various experiments and cross-section microscopy, it was observed that, for such GaN p-FinFET gate structures, the fin packing factor (pitch between fins) and the slope of the sidewall are key factors. Fig. 2.2(g) gives two examples of gate metallization. For poor gate metallization, typically the p-FinFET could not turn off even for a very deep gate recesses (little p-GaN/UID-GaN remaining above AlGaN). RF magnetron sputtering of Ti/Au ($30/50$ nm) was used. Ti was chosen because of its low workfunction (therefore Schottky to p-GaN), and its good adhesion to the SiO_2 surface. Unfortunately, the gate metal could not be too thick because a lift-off technique was used for sputtered metal. A MMA/PMMA layer was used to create a huge undercut (larger than bi-layer

PMMA) which would be advantageous for the lift-off. A detailed description of the process flow is provided in Appendix A.

2.3.2 Results and Discussion

The performance of the p-FET with the best overall characteristics ($L_{SD} = 175$ nm, L_G self-aligned, fin width of 20 nm) is presented in Fig. 2.3. An $I_{D,max}$ of -300 mA/mm, R_{ON} of 27 Ω·mm, and current saturation at high gate overdrive were achieved, as shown in Fig. 2.3(a). The transfer characteristics (Fig. 2.3(b)) reveal a V_{th} of 3 V and a peak transconductance, g_m, of 13 mS/mm. A second g_m peak at large gate overdrive and highly negative V_{DS} likely indicates a second channel being activated, and is investigated in Chapter 4.1. The drain current ON/OFF ratio is 200, limited by the leakage current through the gate dielectric. The hysteresis in the transistor transfer characteristics ($\sim$ 1 V) resembles the hysteresis in metal-SiO_2-metal capacitors (Fig. 2.2(f)), which indicates the significant contribution of the gate dielectric quality (and p-GaN/dielectric interface) and need for further optimization.

The impact of two key device design parameters (fin width, gate recess depth) on DC output characteristics ($I_{D,max}$, R_{ON}) was systematically studied for GaN p-FinFETs. As the fin width is reduced below 50 nm, the current density and R_{ON} improves (Fig. 2.4(a)). However, this trend was not observed above 50 nm, possibly due to the significant reduction in the field-induced acceptor ionization effect [70]. In addition, a deeper gate recess was found to reduce current density (Fig. 2.4(b)), primarily due to reduction of carrier density in the p-channel, but is expected to significantly improve ON-OFF ratio and sub-threshold swing, as is the case for p-FETs based on similar epitaxial structures. Unfortunately, the gate oxide quality in this batch of fabricated transistors was found to be the limiting factor for the current ON-OFF ratio ($< 10^4$). It follows that, the OFF-state characteristics were limited by gate control and drain-induced barrier lowering (DIBL), before a destructive breakdown at $\sim$ 20 V.

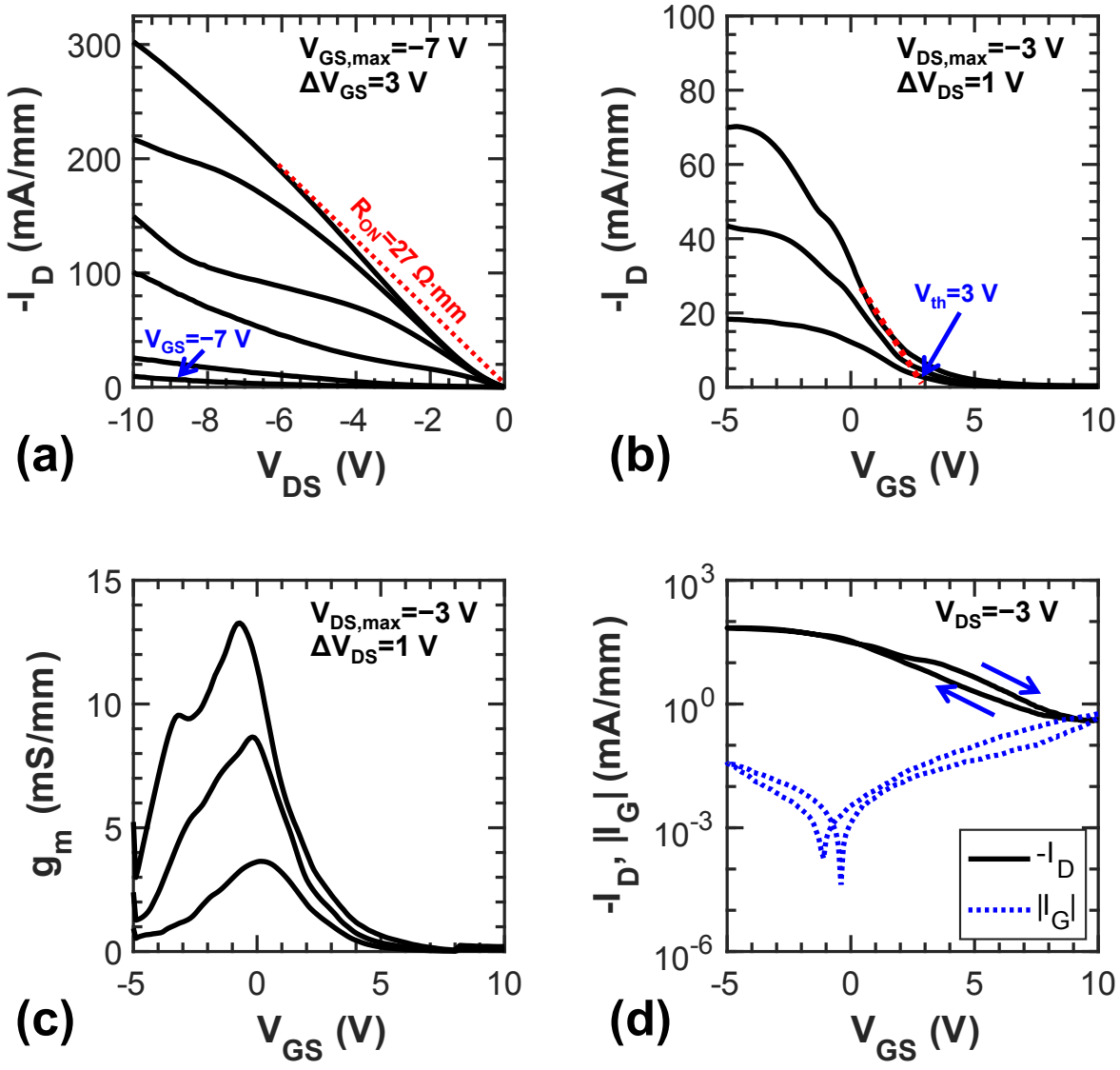


Figure 2.3: Performance of p-FET with $L_{SD} = 175$ nm (L_G self-aligned), fin width= 20 nm. (a) Output characteristics, showing $I_{D,max} = -300$ mA/mm, $R_{\rm ON} = 27$ Ω·mm. Current saturation at higher gate overdrive was observed. Transfer characteristics: (b) Linear I_D *vs.* V_{GS}, showing $V_{th} = 3$ V. (c) Transconductance *vs.* V_{GS}, showing peak $g_m = 13$ mS/mm ($V_{DS} = -3$ V). (d) Logarithmic I_D *vs.* V_{GS}. Current ON/OFF ratio is 200, limited by the gate leakage. The hysteresis is typically attributed to the interface traps at the gate oxide.

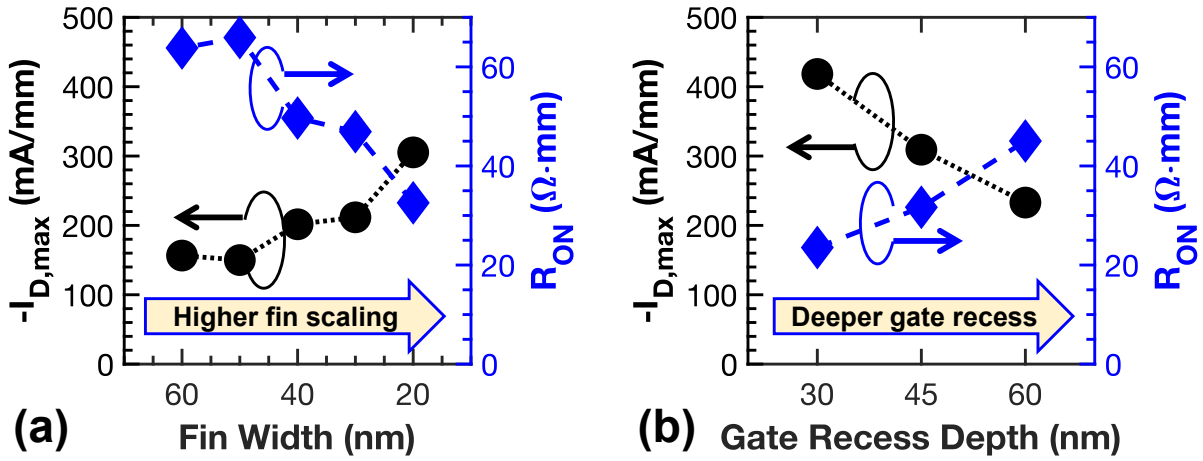


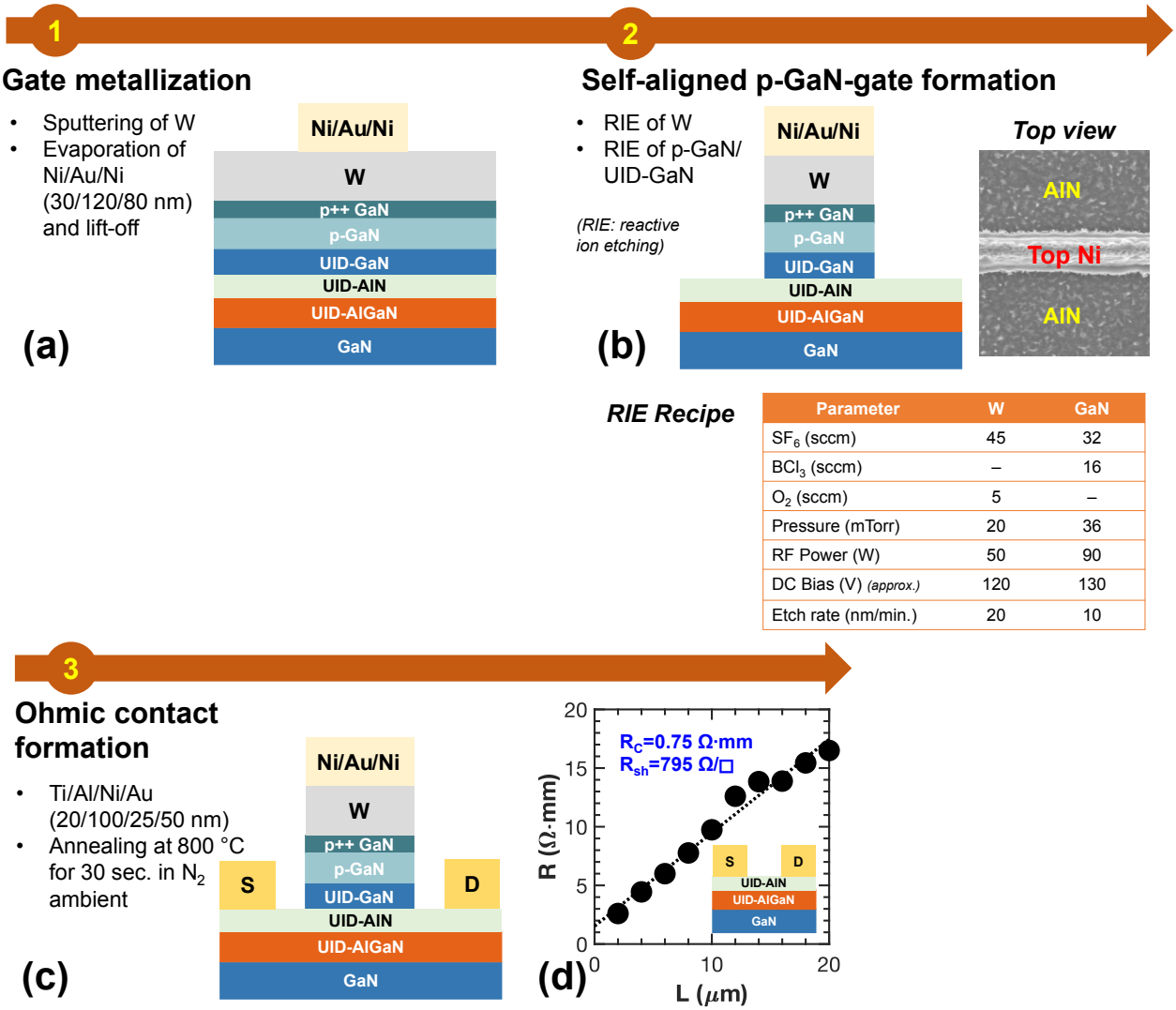
Figure 2.4: Systematic study of the impact of (a) fin width and (b) gate recess depth on the performance ($-I_{D,max}$ and R_{ON}) of GaN p-FinFETs. SA p-FinFETs (~ 40 in total) fabricated in the same batch. $-I_{D,max}$ and R_{ON} were measured at $V_{GS} = -7$ V.

2.4 GaN n-FET

2.4.1 Self-Aligned p-GaN-Gate HEMT Process Flow

Self-aligned p-GaN-gate technologies were previously explored [90, 91]. This work proposes a simple gate-first process flow, which incorporates novel (1) metallization scheme with lower sheet resistance, (2) GaN/AlGaN selective etch recipe, (3) etch hard mask to ensure aggressive scaling of the gate length.

As illustrated in Fig. 2.5, the SA gate process begins with the blank sputtering deposition of W (100 nm). Then, Ni/Au/Ni (30/120/80 nm) was patterned by electron beam lithography and lift-off. W was etched using the top Ni as a hard mask. W was chosen because of its high thermal stability (necessary for a gate-first process) and Schottky behavior with p-GaN gates [65]. p-GaN and UID-GaN (above AlGaN) were etched using SF_6/BCl_3. The optimization of the epitaxy and selective etch will be explained next. Lastly, ohmic contacts were formed by Ti/Al/Ni/Au alloyed at 800 °C in N_2 ambient. The typical contact resistance is ~ 0.75 Ω·mm, which could be further optimized for contact formation through the AlN/AlGaN barrier. A fabricated scaled



Parameter	W	GaN
SF_6 (sccm)	45	32
BCl_3 (sccm)	–	16
O_2 (sccm)	5	–
Pressure (mTorr)	20	36
RF Power (W)	50	90
DC Bias (V) *(approx.)*	120	130
Etch rate (nm/min.)	20	10

Figure 2.5: Process flow of self-aligned W/p-GaN-gate n-FET: (a) Conformal deposition of W, then patterning of Ni/Au/Ni (30/120/80 nm) using electron beam lithography and lift-off. (b) Self-aligned (SA) p-GaN gate formation is achieved using reactive ion etching (RIE) of W and GaN (recipes are included). AlN layer aids the etch stop to minimize damage to the n-channel. (c) Formation of ohmic contacts using alloyed Ti/Al/Ni/Au. (d) TLM measurement of ohmic contacts. In the SA p-GaN-gate, the extent of the p-GaN region is defined by the top Ni/Au/Ni.

SA p-GaN-gated n-FET is presented in Fig. 2.1(d). A detailed description of the process flow is provided in Appendix A. A proof-of-concept layout was adopted, where the fabricated n-FETs are symmetric (gate is located in the center of the ohmic contacts, or $L_{GS} = L_{GD}$), and that electric field management structures (e.g. edge termination) were not included.

It is evident that an important step for the p-GaN HEMT is the selective etch, where the p-GaN is selectively removed over AlGaN, or in other words, the etch stops at the AlGaN layer. This step is in between the steps in Fig. 2.5(a)–(b). The purpose is to completely remove the p-GaN in the ohmic regions (for formation of ohmic contact to AlGaN/GaN 2DEG) and in the access regions (to recover the 2DEG from the depletion by p-GaN). Any remaining p-GaN (incomplete etch) would lead to an increase in access resistance or the poor performance of ohmic contacts. Furthermore, if a conventional Cl-based etch for III-N were to be used, the etch has little selectivity between GaN and AlGaN, therefore the etch would need to be perfectly timed to ensure the etch stops on AlGaN. Such a recipe requires very careful calibration of the etch rate, and more importantly, is not robust to variations in p-GaN thickness across the sample, variation in local etch rate across the sample etc. Instead, the selective etch relies on achieving an "etch stop" layer at the AlGaN top surface.

Fig. 2.6(a) explains the concept of a selective etch, from a fabrication perspective. The etch chemistry needs to be able to etch GaN, but effectively form an "etch stop" layer. In this work, BCl_3/SF_6 plasma was used, which has been reported to give high etch selectivity [92]. To the first order, BCl_3 etches GaN, while SF_6 allows for the formation of non-volatile AlF_x (not possible during etching of GaN). Selective etching of p-GaN over AlGaN was achieved using BCl_3/SF_6 plasma, which has been reported to give high etch selectivity [92].

In the former GaN-CMOS platform, the selective etch would resemble the schematic shown in Fig. 2.6(b), where the shaded region denotes the etched p-GaN/UID-GaN through the selective etch process. In order to achieve a better etch stop at the AlGaN layer, a UID-AlN layer (in actual implementation in MOCVD, $Al_xGa_{1-x}N$ with $x > 0.8$ layer is inserted in the GaN-CMOS epitaxy of this work. In the case of the selective etch recipe used, the F (from plasma) forms a non-volative AlF_x layer, therefore effectively creating an etch stop. An AlGaN layer with a higher Al

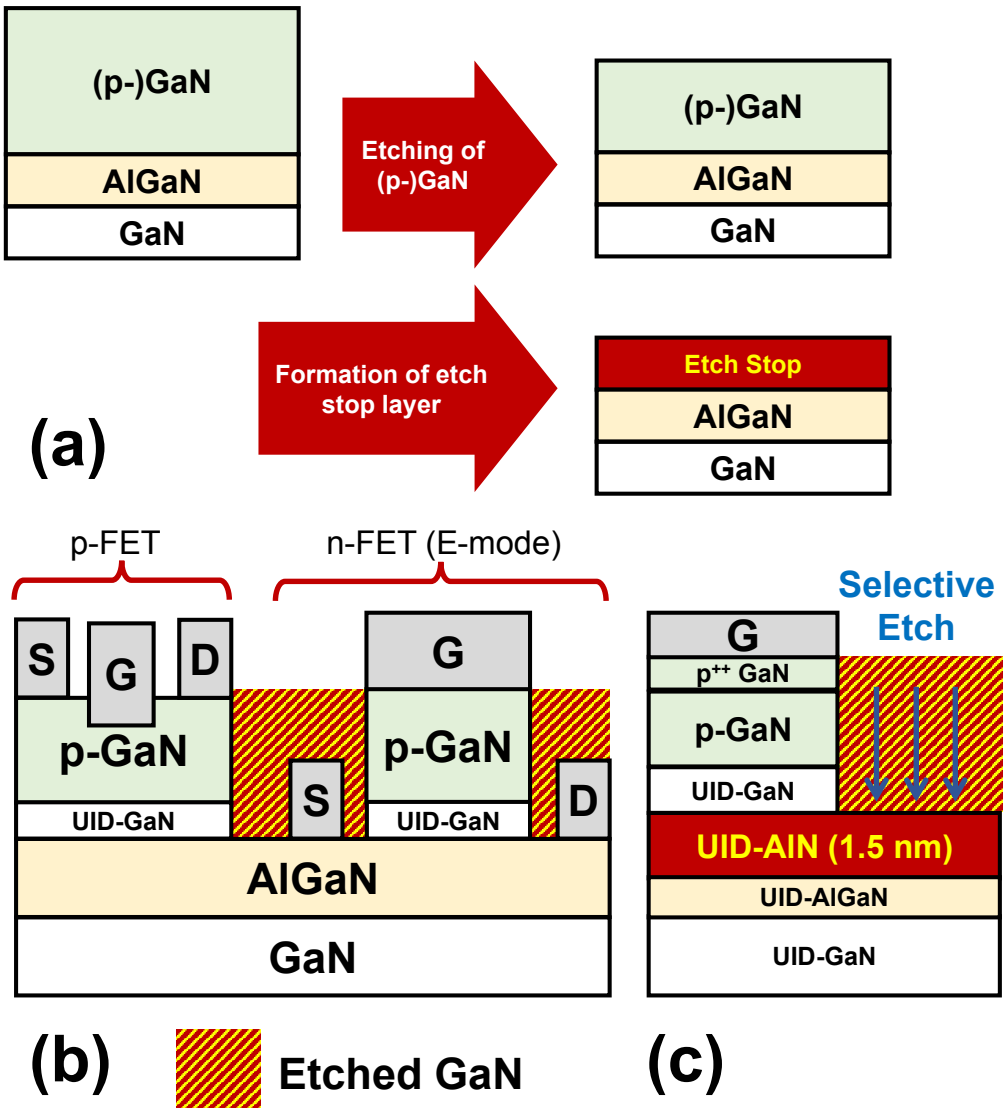


Figure 2.6: Selective etch for fabrication of n-FET. (a) Schematic of GaN-CMOS platform (former epitaxy) with p-FET and n-FET, showing the selectively etched p-GaN/UID-GaN region. (b) Epitaxy of this work which incorporates a UID-AlN (1.5 nm) layer.

composition would allow for the more effective creation of an etch stop, as shown in Fig. 2.6(c).

Significant optimization was required to realize the proposed SA p-GaN-gate process, as illustrated in Fig. 2.7(a). The use of a Ni/Au/Ni metal stack allows for, (1) the top Ni to serve as the hard mask for gate definition; (2) the reduction of gate sheet resistance from 10 $\Omega/\square$ (W only) to < 0.5 $\Omega/\square$ (this work). It was found to be difficult to deposit the entire W/Ni/Au/Ni stack using a single evaporation and lift-off step. Therefore, two metal deposition steps were required. Two aspects are critical for the gate module, namely (1) a highly selective GaN/AlGaN etch with good surface morphology after etch; (2) highly robust etch mask using gate metal for the etch in (1). Fig. 2.7(b) presents short-loop tests of GaN/AlGaN selective etch, which indicate $> 10:1$ selectivity and rms roughness of 6 nm. Next, the top metal mask was integrated with this selective etch recipe. Careful optimization was required to the etch conditions and mask. A poor etch would result in significant re-deposition of particles around the gate structure (Fig. 2.7(c)). Furthermore, considering the degradation of the gate structure (Fig. 2.7(d)), such a transistor would require greater access region lengths (L_{GS} and L_{GD}) than what is required for lithography alignment tolerance of the ohmic contacts (as is the case of a standard HEMT). The optimized gate structure is presented in Fig. 2.7(e)–(f). A 80 nm-thick layer of Ni was required in order to ensure sufficient etch resistivity against both F-based and Cl-based plasmas.

2.4.2 Results and Discussion

Scaled n-FETs with $L_G = 200$ nm, $L_{SD} = 1.1$ µm show good current saturation with $I_{D,max} = 525$ mA/mm, $R_{ON} = 2.9$ Ω·mm (Fig. 2.8(a)). E-mode operation with $V_{th} \approx 1.6$ V was achieved (Fig. 2.8(b)). A peak g_m of 265 mS/mm reflects good gate control using the proposed gate metallization stack. As expected, gate length scaling improves $I_{D,max}$ for the ON-state characteristics, but slightly worsens the gate control in the OFF-state breakdown measurements. The destructive breakdown was ~ 50 V. It should be noted that, none of the transistors in this work feature any electric field management structures (e.g. field plates, charge balancing [93]), which are expected to push the boundary of the $R_{ON,SP} \times$ BV trade-off. ($R_{ON,sp}$ is normalized by area, also known as $R_{ON} \times A$.)

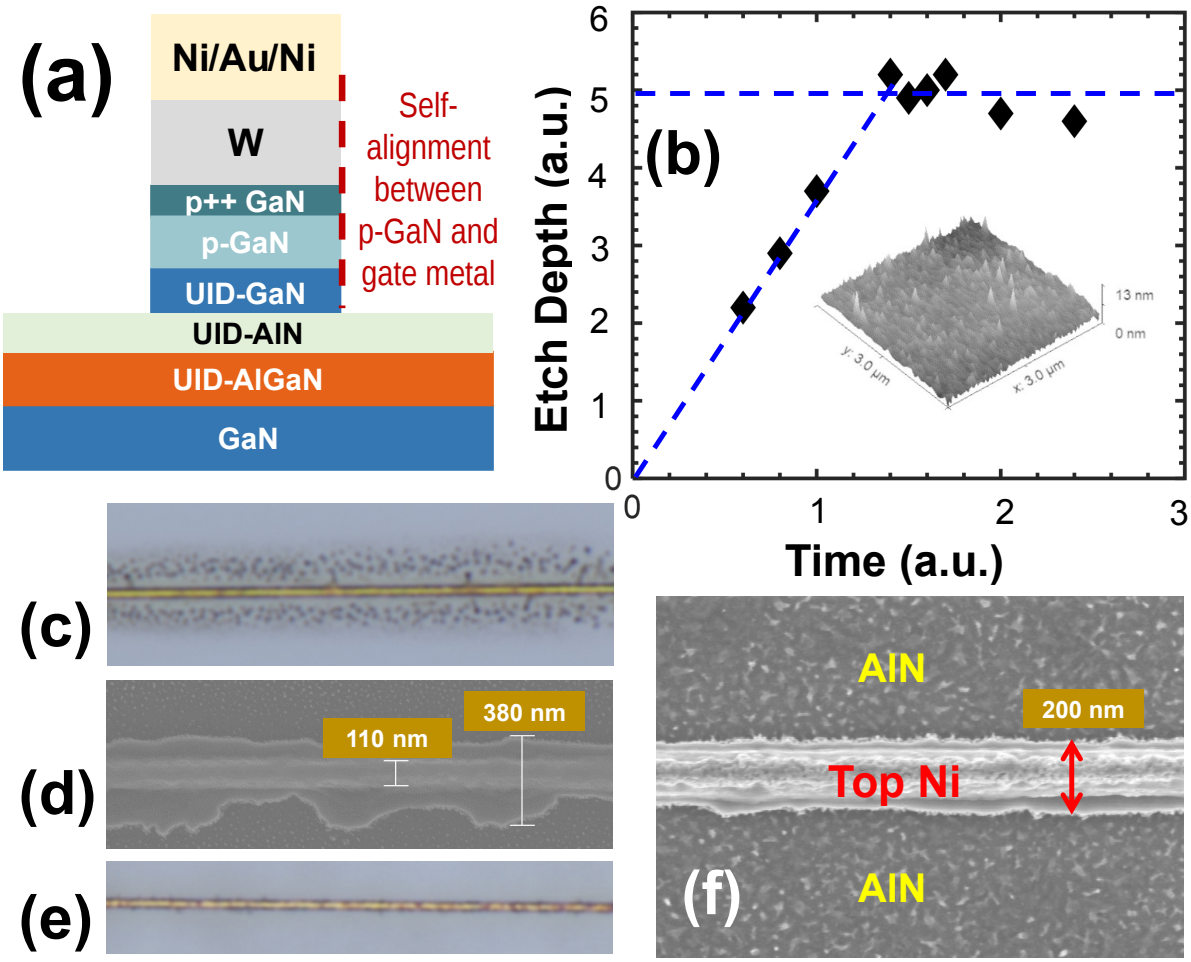


Figure 2.7: Details of fabrication optimization of n-FET (p-GaN-gated AlGaN/GaN HEMT), with particular attention on the novel SA p-GaN-gate. (a) Device structure after the formation of the SA p-GaN-gate. (b) Selective etch of p-GaN over AlGaN using a BCl_3/SF_6 process. The inset illustrates the morphology of the etched surface showing an rms roughness of 6 nm. (c) Optical image of a gate region (but with thin top Ni mask), showing that significant amounts of metal was sputtered off the gates. (d) SEM image of a gate with a non-ideal etch. (e)–(f) Optical and SEM images of a gate region with optimized etch, respectively. The region around the gate metal was clean.

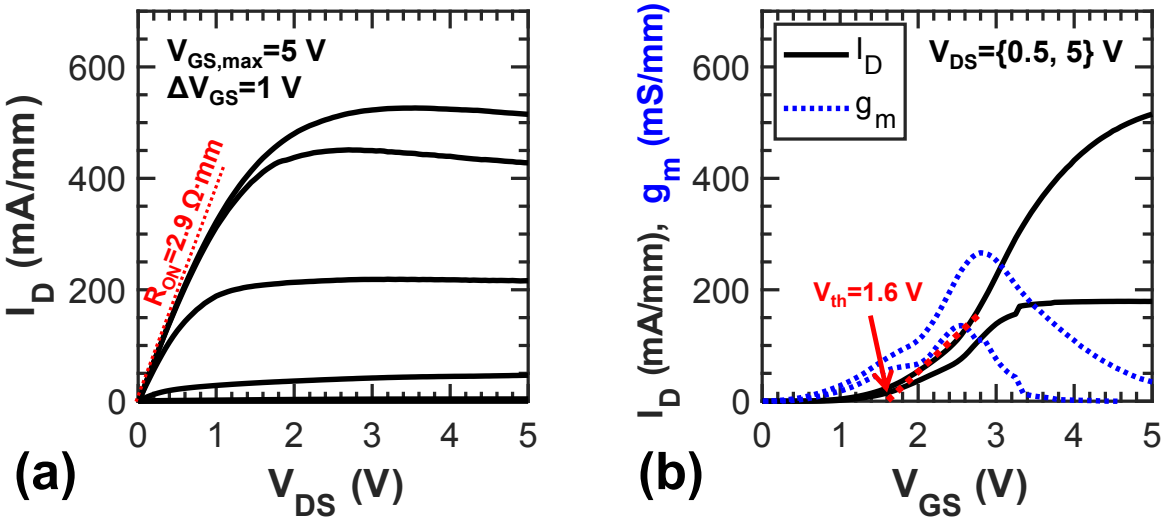


Figure 2.8: Performance of n-FET with $L_G = 200$ nm, $L_{SD} = 1.1$ µm fabricated on Epi-1. (a) Output characteristics, showing $R_{ON} = 2.9$ Ω·mm and good current saturation with $I_{D,max} = 525$ mA/mm (calculated at $V_{GS} = 5$ V). (b) Transfer characteristics, showing $V_{th} = 1.6$ V and peak $g_m = 265$ mS/mm.

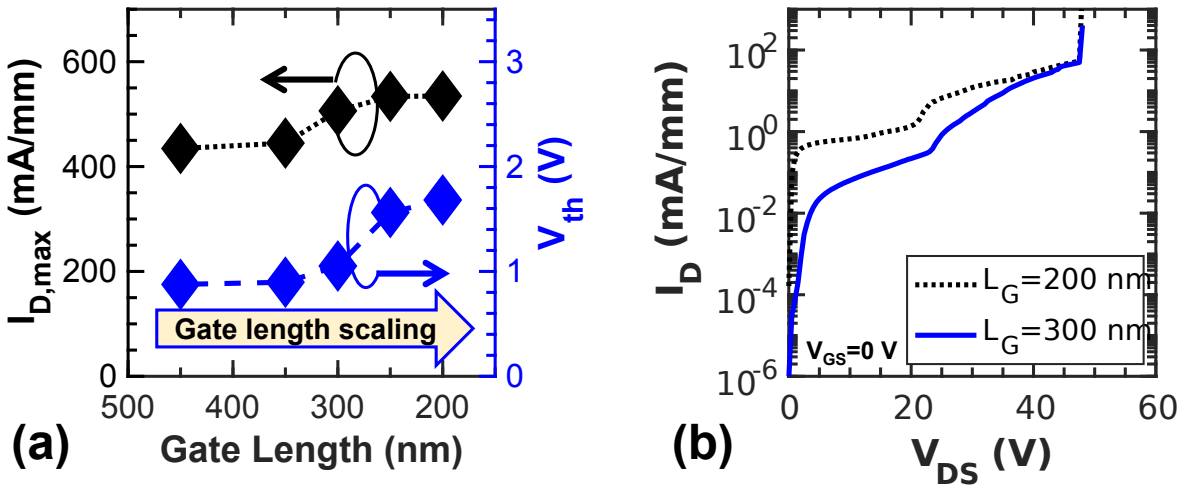


Figure 2.9: Gate length scaling of SA p-GaN-gate n-FETs (Epi-1). (a) ON-state characteristics. ~ 40 transistors fabricated in the same batch were studied. (b) OFF-state characteristics, without any electric field management structures (e.g., field plate). In these transistors, $L_{GS} = L_{GD} = 450$ nm.

As shown in Fig. 2.9, the impact of gate length scaling on the SA p-GaN-gate n-FETs was studied. In terms of ON-state characteristics, gate length scaling improves $I_{D,max}$. Furthermore, it is observed that V_{th} becomes more positive (E-mode) for scaled $L_G < 250$ nm. In terms of OFF-state characteristics, a slightly longer L_G improves gate control and reduces leakage current before destructive breakdown (at ~ 50 V). It should be noted that, none of the transistors in this work feature any electric field management structure.

The maximum achievable I_D in the W/p-GaN-gate HEMTs is typically limited by (1) the allowable gate overdrive before the onset of significant gate leakage; (2) carrier velocity in scaled transistors. Through analysis of temperature-dependent current-voltage characteristics from room temperature to 500 °C, it was found that the gate current in the reverse bias and onset of forward bias is dominated by two-dimensional variable range hopping (2D-VRH), while the gate current in the strong forward bias regime is dominated by the leakage through the vertical junction current. A detailed analysis of the gate leakage of such W/p-GaN-gate HEMTs (including temperature dependency) is reported in [94].

2.4.3 Comparison of n-FETs based on the GaN-CMOS platform and a conventional p-GaN epitaxy

As mentioned in Sect. 1.3, there are some noticeable differences between the GaN-CMOS platform and the conventional p-GaN HEMT epitaxy. While the exact epitaxial design of commercially available p-GaN-HEMTs are not publicly known, a conventional p-GaN HEMT epitaxy (Fig. 1.2(a), p-GaN (70 nm)/AlGaN (15 nm)/GaN, "Epi-2") was used for this experiment. While the scaled SA p-GaN-gate n-FET technology was originally developed for integration with p-FETs on the GaN CMOS platform, it could also be useful in its own in low-voltage GaN power ICs or GaN n-FET-only logic. To evaluate the robustness of this technology for such a possibility, the same process flow was applied on a conventional p-GaN-gate epitaxial structure. It should be noted that, previous efforts have been made to fabricate p-FETs on Epi-2 [95].

In the n-FETs based on Epi-2, better performance ($I_{D,max} = 750$ mA/mm, $R_{ON} = 1.3$ Ω·mm),

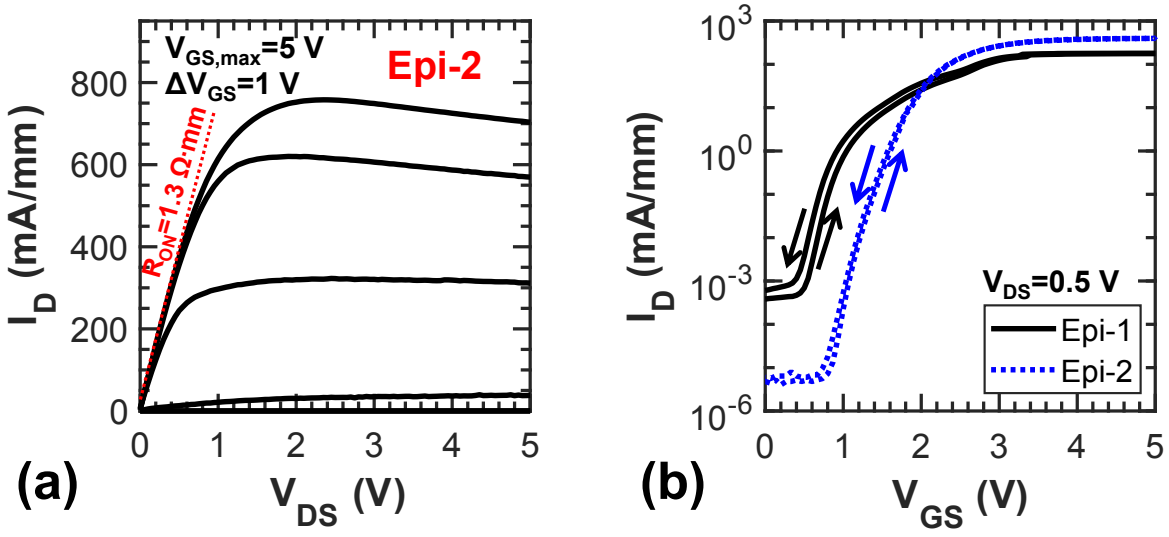


Figure 2.10: Performance of n-FET fabricated on Epi-2. (a) Output characteristics, showing $R_{ON} =$ 1.3 Ω·mm and good current saturation with $I_{D,max} = 750$ mA/mm (calculated at $V_{GS} = 5$ V). (b) Comparison of the performance of n-FETs based on Epi-1 and Epi-2.

higher current ON-OFF ratio (Fig. 2.8(c)), sharper ON-OFF transition (*SS* values of n-FETs based on Epi-1 and Epi-2 are 123 mV/dec and 100 mV/dec, respectively), and negligible hysteresis (< 0.1 V)) (Fig. 2.8(d)) were observed. The above improvements with respect to the n-FET in the CT platform are attributed to the location of the gate metal closer (by ~ 25 nm) to the n-channel at the AlGaN/GaN interface, and better gate electrostatic control by the metal gate to the n-channel (absence of UID-GaN and AlN, thinner AlGaN layer).

Here, two issues are discussed in these n-FETs (p-GaN-gate HEMTs). Firstly, the use of a gate structure where the gate metal (W-based) and p-GaN are self-aligned. The advantage is that this method allows for aggressive channel length scaling, because there would not need to be lithography tolerances between the gate metal and the p-GaN. However, some reports have suggested that this self-alignment results in reliability issues, and that a non-self-aligned gate metal/gate (gate metal is smaller than p-GaN) would be desired from a reliability perspective [96]. For example, it is reported that, recoverable negative V_{th} shifts and permanent degradation have seen to occur mostly in the proximity of the gate edge [97]. The gate leakage through the sidewall of p-GaN

(and gate breakdown) could be suppressed by a non-self-aligned metal/p-GaN structure [98]. Furthermore, the reported experiments were done on conventional p-GaN epitaxies (similar to Epi-2); issues would need to be addressed in the context of the GaN-CMOS platform (Epi-1), in order to evaluate the reliability issues in the proposed scaled GaN n-FETs.

Secondly, while both Epi-1 and Epi-2 feature an approximate p-GaN/AlGaN/GaN heterostructure, the p^{++} layer in Epi-1 makes the same gate metal more ohmic (less Schottky) to the p-GaN island. W, with a low workfunction of 4.5 eV) is chosen, is potentially the lowest workfunction among refractory metals (with the next lowest being Mo). Note that refractory metals are required for the first metal layer so that they can survive the RTA in the subsequent ohmic step. W has been used in p-GaN HEMTs and p-FETs [65, 99]. Therefore, for Epi-1, the gate resembles more of the ohmic gate type of p-GaN HEMT. One recalls the equation

$$p = N_v \exp\left(\frac{E_v - E_F}{kT}\right) \tag{2.1}$$

where p is the hole concentration, N_v is the effective density of states in the valence band, E_v and E_F are the valence band energy and Fermi level, respectively, and kT is the product of the Boltzmann constant and the temperature. One assumes that only the p changes and the other variables remain constant (e.g., constant activation ratio of Mg). Then, for a $2\times$ increase in p, the value of $E_v - E_F$ decreases by $(\ln 2 \approx 0.693)$ eV. This decrease is translated to a decrease in the Schottky barrier height by the same amount. Of course, other effects such as Fermi-Level pinning at the gate metal/p-GaN interface would need to be considered, but this is an experimental phenomenon highly dependent on the surface treatment, and post gate annealing [100].

There are different design considerations (and implications in transistor characteristics and reliability) for ohmic-gate p-GaN-gate HEMTs. These would need to be carefully considered in future work.

2.5 Benchmarking

Fig. 2.11(a) summarizes the performance of GaN p-FETs in terms of two key device-level parameters, $-I_{D,max}$ and $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$. To the best of the author's knowledge, the best p-FET in this work feature the highest current density among MOCVD III-N p-FET ($> 2\times$ the previous record, -140 mA/mm [61]), as well as competitive performance compared with GaN/AlN molecular beam epitaxy (MBE) counterparts [54]. Fig. 2.11(b) plots $-I_{D,max}$ *vs.* V_{th}, showing that the proposed p-FETs are closed to the desired corner. In general, E-mode operation ($V_{th} < 0$ V for p-FETs) is desired for power ICs. It is observed that most of the high current density p-FETs are D-mode, with one reason being the higher allowable gate overdrive, and another reason being that D-mode p-FETs have higher total charge in the channel (refer to Chapter 4).

As presented in Fig. 2.11(c), the maximum current density of p-FETs was plotted against gate length to study the impact of (aggressive) channel length scaling, which is one of the main objectives of this work. The p-FET of this work achieved $-I_{D,max} \times L_G = 52.5$ μA, which is a record for MOCVD-based (single GaN/AlGaN epitaxial layer) p-FETs, and is close to the values for the record MBE-based p-FETs and MOCVD super-lattice (multiple GaN/AlGaN epitaxial layers) p-FETs. Two observations may be made. (1) The p-FETs with the highest current densities feature ultra-scaled gate lengths < 200 nm. This observation is in agreement with previous p-FET reports on gate length scaling of a single type of p-FET [65]. (2) To achieve substantial improvement from the state-of-the-art $-I_{D,max} \times L_G$ values, new epitaxial structures and better quality growth would be highly desired. In addition to the benchmarking of Fig. 2.11, it is worthy to note that, the proposed p-FET technology is compatible with n-FETs fabricated on the same GaN-on-Si platform, as indicated by the solid symbols in these figures.

The n-FET is a p-GaN-gate HEMT, where significant research has been conducted, mainly for medium and high voltage > 200 V switching applications, as shown in Fig. 2.12. There are a few reports of lower voltage demonstrations, mainly targeting power ICs and RF operation. To the best of the author's knowledge, at the time of publication, the reported n-FET p-GaN HEMT

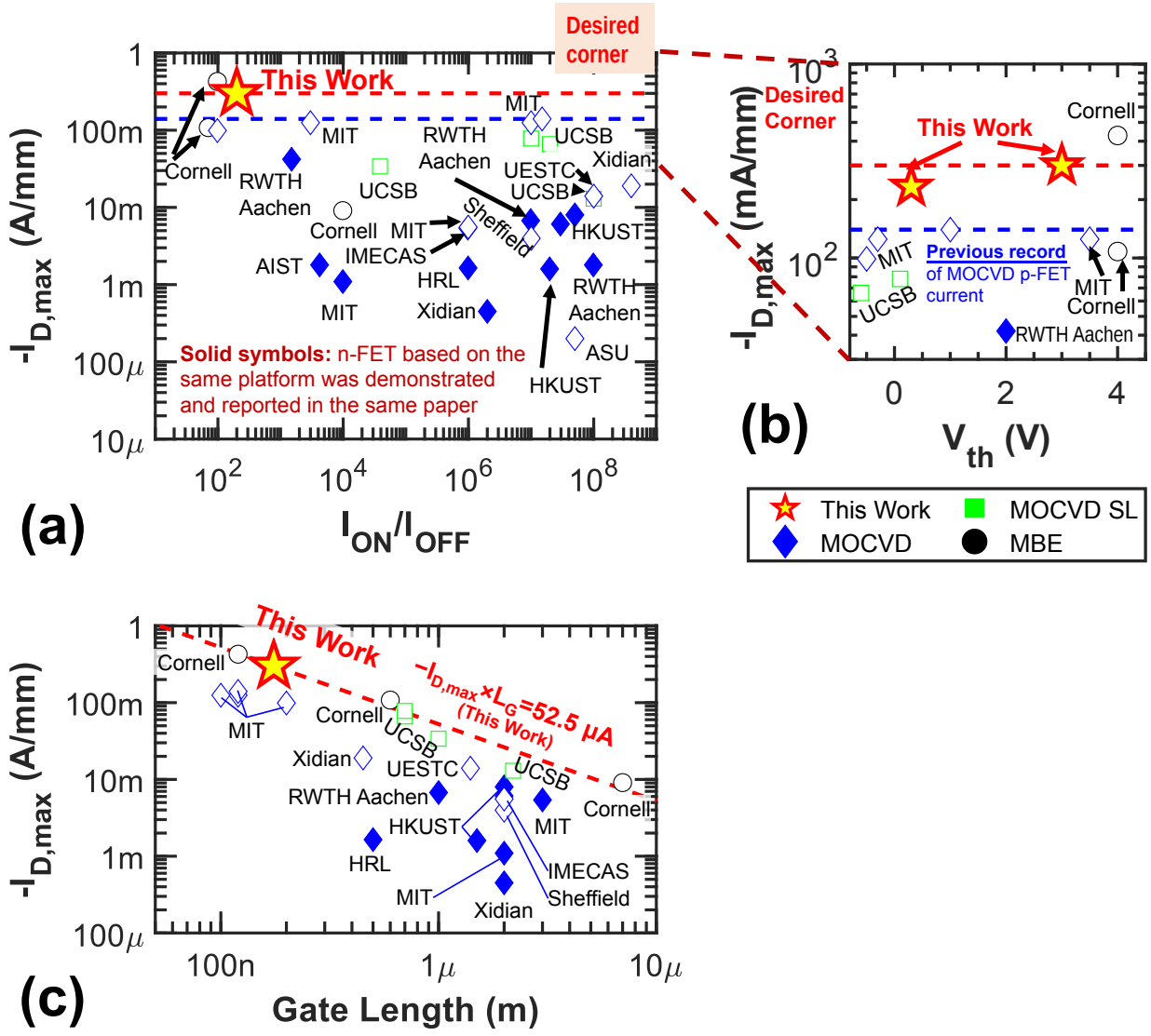


Figure 2.11: Benchmarking of GaN p-FET. (a) ON-current and ON-OFF ratio. The two best p-FETs in this work show competitive performance compared with the existing MBE p-FET. (b) A zoom-in of the p-FETs with higher ON-current and a comparison of V_{th}. (c) GaN p-FETs taking into account the trade-off between current density and gate length.

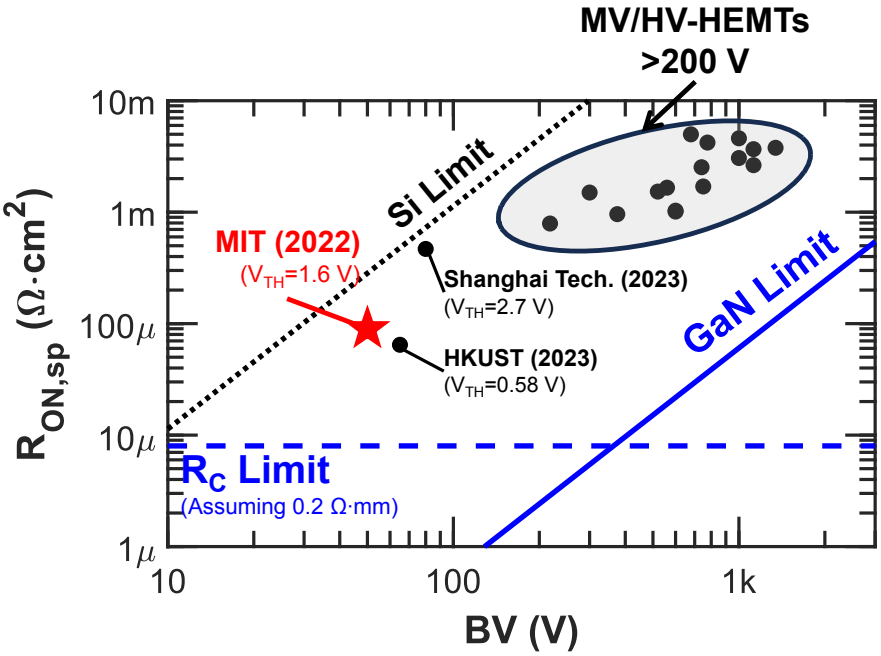


Figure 2.12: Benchmarking of ON *vs.* OFF characteristics of the n-FET (Epi-1, GaN-CMOS platform) with E-mode p-GaN-gate HEMTs reported in the literature. Given that in most lateral transistors, the resistance is normalized by transistor width, $L_T = 1$ μm is assumed, and $2 \times L_T$ is added to the L_{SD} as the best-case approximation.

(Epi-1) was an early work and showed a good combination of $R_{ON,sp}$ and breakdown voltage, and follows the "trade-off" of these two parameters, which represent ON and OFF-state characteristics, respectively. As compared to similar works later reported, the n-FET of this work maintained strong E-mode ($V_{th} = 1.6$ V). It is worth noting that, this p-GaN-HEMT was fabricated on the GaN-CMOS platform (Epi-1) (not the conventional p-GaN platform), therefore indicating the promise of the proposed GaN-CMOS platform for power ICs. Future work may be conducted on lower voltage n-FETs, which would target high speed power and mixed-signal ICs. Of course, there is a R_c limit to the scaling, which would be the bottleneck rather than the intrinsic GaN material limit (Baliga's figure of merit). An initial attempt of n-FETs using the GaN-CMOS platform exceeds the Si limit, therefore also indicating the promise of GaN-CMOS for lower voltage applications (currently dominated by Si-LDMOS technology [101]).

A benchmarking of GaN CT based on the same platform was performed, as presented in Fig. 2.13. All of the reports of n-FETs and p-FETs based on the same platform (i.e. reported in a single

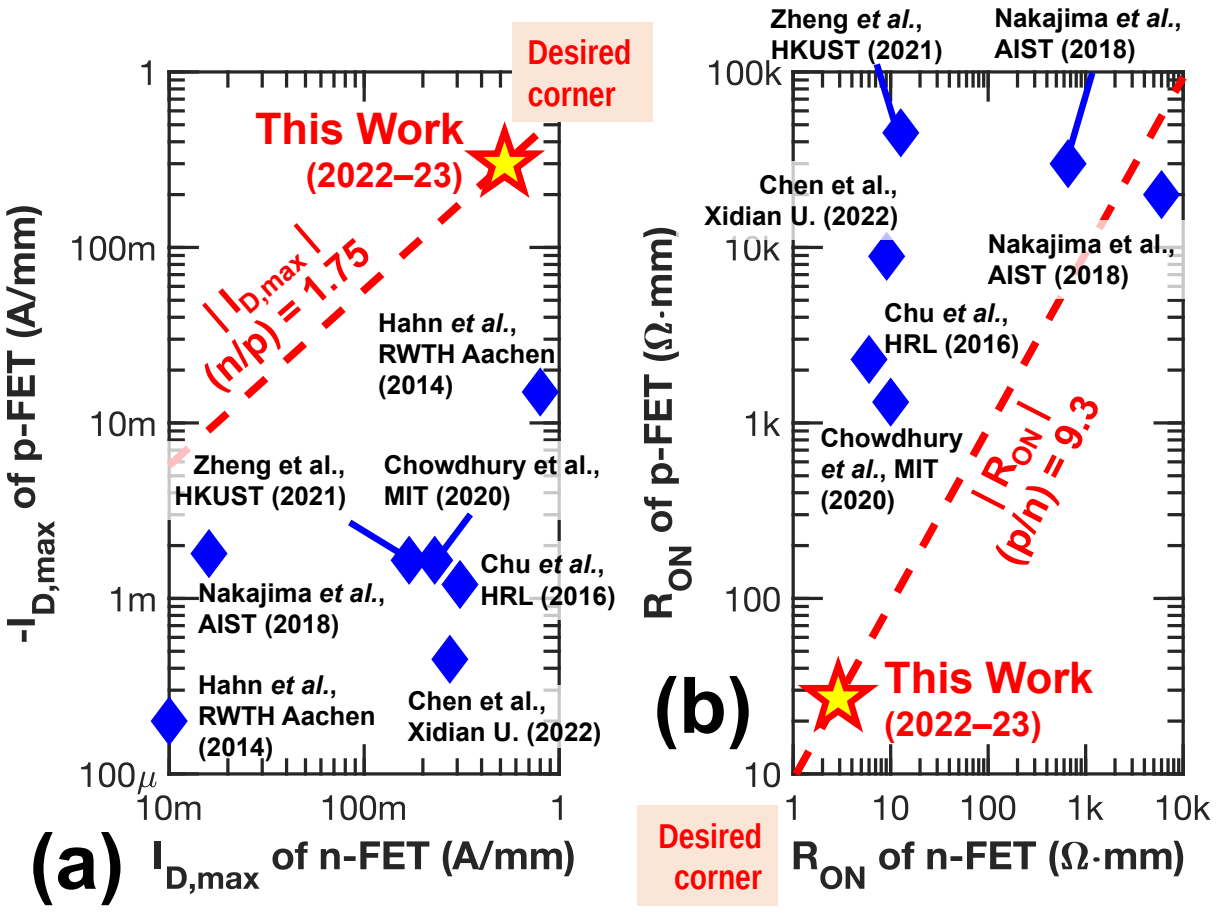


Figure 2.13: Benchmarking of GaN CT demonstrations (complementary transistors reported in the same paper) based on $|I_{D,max}|$ and R_{ON}. (a) Maximum current density (drive current) of p-FET *vs.* n-FET. (b) R_{ON} of p-FET *vs.* n-FET.

publication) are based on MOCVD-grown epitaxial structures [11, 26, 27, 51, 52, 102, 103]. The results of the benchmarking are graphically presented in Fig. 2.13, while more detailed information is presented in Table 2.1. Two parameters, namely $|I_{D,max}|$ (ratio of n-FET/p-FET, Fig. 2.13(a)) and R_{ON} (ratio of p-FET/n-FET, Fig 2.13(b)), are highlighted because of their significance in power and digital IC design. A ratio approaching unity ($= 1$) is desired to achieve reasonable transistor sizing. The current density of the reported GaN CT is comparable with that of 5 V-rated Si CMOS in an industry 0.13 µm BCD process published in 2016 ($I_{D,max\{n,p\}} = \{520, -323\}$ mA/mm) [104].

Fig. 2.13 and Table 2.1 reveal that significant advancement in the performance of GaN CT has been achieved over the years. This work continues to push the performance of GaN CT, as compared to other reports and the authors' earlier demonstration in 2020 [26], thanks to innovation in device architecture (self-alignment), aggressive scaling, and optimization of processing technology. These results were achieved despite relatively high channel resistances ($R_{sh\{p,n\}} \approx \{60000, 800\}$ Ω/□), which could be improved with optimization of epitaxial design.

It is noted that, a disparity between the ratios of $|I_{D,max}|$ and R_{ON} exists. This phenomenon is attributed to several reasons, mainly related to the characteristics of the p-FET: (1) Schottky turn-on behavior of the p-FET; and (2) significant field-induced acceptor ionization at high gate overdrives and highly negative drain biases, in particular for the FinFET structure, as explained in Section 2.3.2. Finally, it should be acknowledged that, significant research remains to be done in the co-optimization of this emerging GaN CT in (1) further advancement of various process modules, e.g. ohmic contacts with low contact resistance [105–107], low damage gate recess [65, 70]); (2) device and process engineering to achieve a good balance of performance specifications (DC and switching characteristics); and (3) epitaxial structure, to achieve lower channel resistances while ensuring carrier confinement.

Table 2.1: Benchmarking of GaN CT demonstrations based on $|I_{D,max}|$ and R_{ON}.

Affiliation	**Year**	**Epitaxial Structure**	**Substrate**	$\|I_{D,max}\|$ **[mA/mm] (n/p-FET)**	R_{ON} **[Ω·mm] (p/n-FET)**	V_{th} **[V] (n/p-FET)**
RWTH Aachen [51]	2014	p-GaN/GaN/AlInGaN/GaN	Sapphire	$10/0.2 = 500$	–	$0.5/-0.5$
				$800/15 = 53$	–	$-11/2$
AIST [52, 102]	2015	p-GaN/GaN/AlGaN/GaN	Sapphire	$16/1.8 = 8.8$	$30000/660 = 45$	$-2/4$
	2018	p-GaN/GaN/AlGaN/GaN	Sapphire	$0.14/0.01 = 14$	$20000/6000 = 3.3$	$4/-2.7$
HRL [11]	2016	(1) AlGaN/GaN (2) p-GaN/ GaN/AlGaN (regrowth)	Sapphire	$230/1.65 = 140$	$1314/10 = 131$	$0/0$
MIT [26]	2020	p-GaN/GaN/AlGaN/GaN	Si	$310/1.2 = 258$	$2300/6 = 383$	$0.2/-1$
HKUST [27]	2021	p-GaN/AlGaN/GaN	Si	$170/1.65 = 103$	$4500/12.7 = 354$	$2.5/-2$
Xidian U. [103]	2022	p-GaN/AlGaN/GaN	Si	$275/0.45 = 611$	$8900/9.1 = 978$	$2.3/-2$
This Work	**2022**	**p-GaN/GaN/AlN/AlGaN/GaN**	**Si**	$\mathbf{525/300 = 1.75}$	$\mathbf{27/2.9 = 9.3}$	$\mathbf{1.6/3}$

Values, if not reported directly in the respective papers, are based on best estimates from the published data. Epitaxial layers are unintentionally doped (UID) unless otherwise stated.

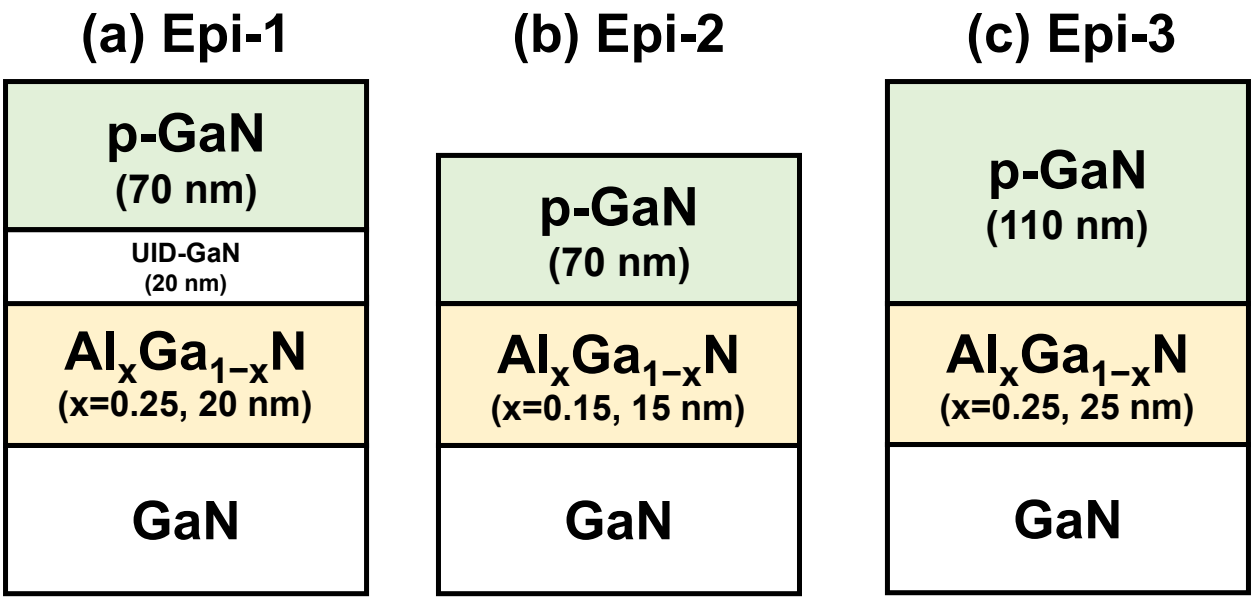


Figure 2.14: Epitaxial structures used in the process development of ICP-RIE selective etch. (a) and (b) correspond to Epi-1 and Epi-2, respectively. (c), or Epi-3, is a p-GaN/AlGaN/GaN epitaxial structure with a similar p-GaN growth as a commercial p-GaN wafer.

2.6 Development of Improved GaN/AlGaN Selective Etch Recipe

As illustrated in Fig. 2.6, the GaN/AlGaN selective etch is an important process for the n-FET (p-GaN-gate HEMT). Furthermore, other E-mode transistor designs which rely on AlGaN/GaN heterostructure (e.g. MIS recessed gate HEMT [108], AlGaN/GaN FinFET [79]) could also be fabricated on the GaN-CMOS platform, but all of these processes depend heavily on the selective etch. The selective etch process reported in Fig. 2.5(b) uses a Reactive Ion Etching (RIE) tool. Given the latest trends of moving towards Inductively Coupled Plasma (ICP)-RIE, for future fabrication, a recipe based on ICP-RIE would need to be developed. Note the distinction between ICP-RIE and RIE, in that the ICP RF power source is separate. Thus, in ICP-RIE technology, the process window is enlarged (because of decoupling between the ion current and ion energy), especially in terms of ensuring high selectivity [109].

This work uses several epitaxial structures, which are all based on GaN/AlGaN/GaN, but with different thicknesses of top GaN and AlGaN, and different alloy compositions in AlGaN, as illustrated in Fig. 2.14.

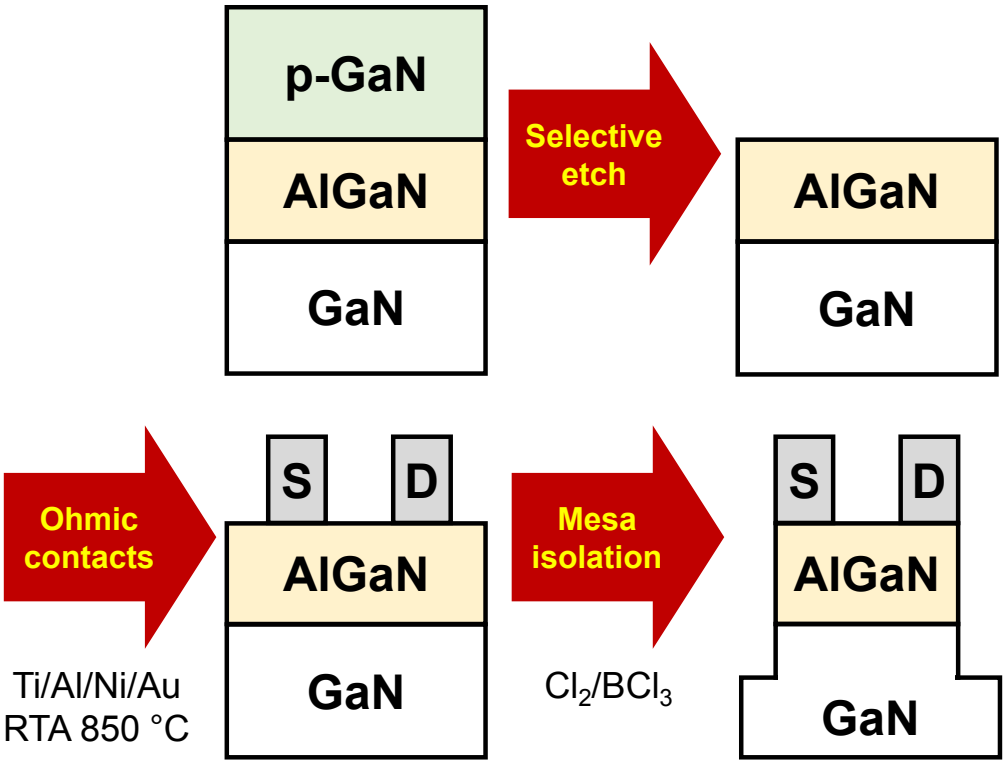
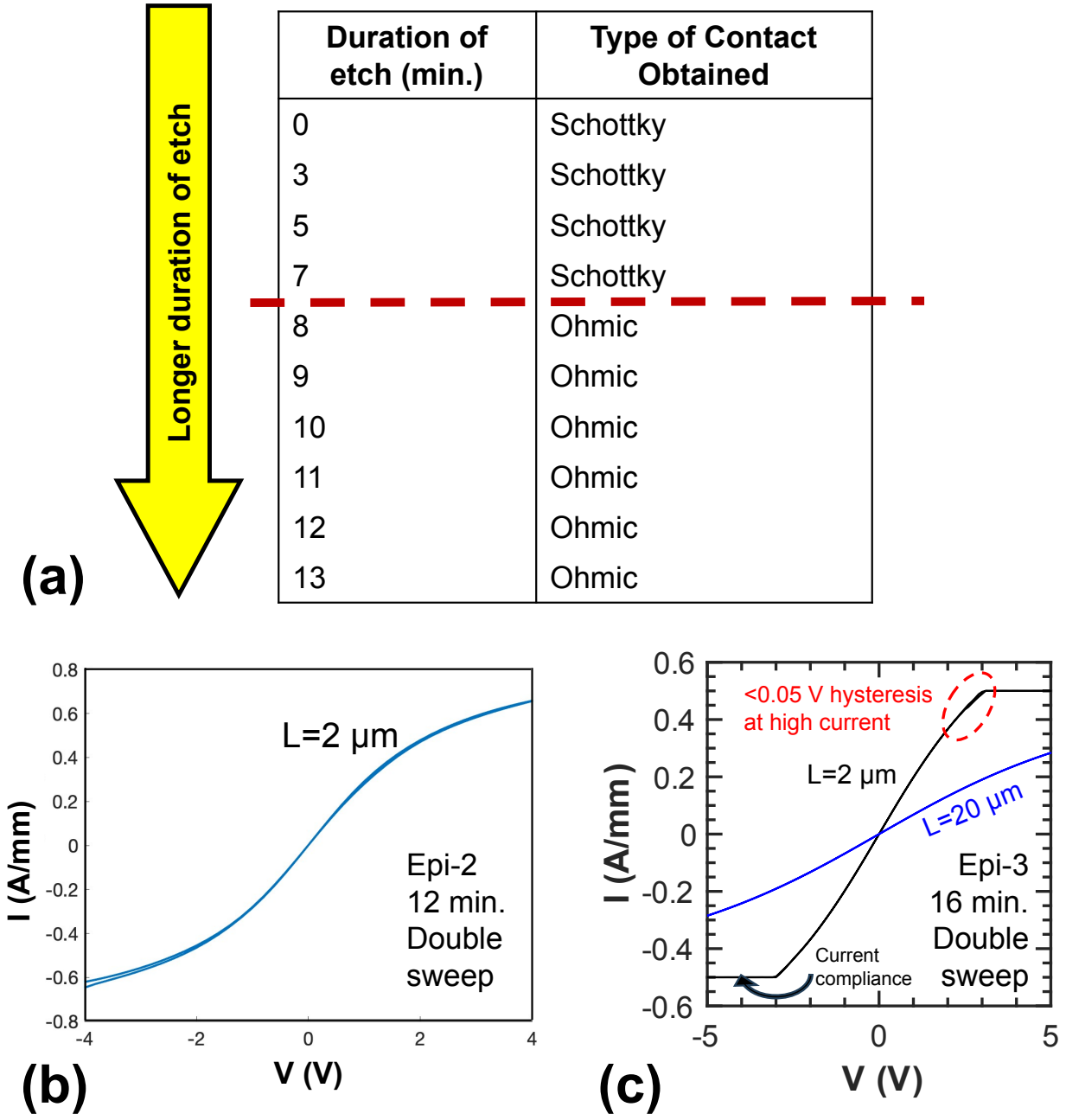


Figure 2.15: Process flow used in the development of the ICP-RIE selective etch. After the selective etch step, alloyed ohmic contacts are fabricated.

The process development of the selective etch using the original RIE recipe was heavily reliant on characterizing the etch depth (using atomic force microscope (AFM)), as shown in Fig. 2.7(b). However, a major issue is that the AFM scans could be affected by local surface morphology, or non-uniformity in the p-GaN thickness across the sample. On the other hand, in the initial process development (finding the process window) for the ICP-RIE selective etch recipe, a process flow which focuses on achieving good ohmic contacts was used (Fig. 2.15). This resembles the actual process flow for the formation of n-FET ohmic contacts (to AlGaN/GaN 2DEG). After the selective etch step, alloyed ohmic contacts are fabricated. A Ti/Al/Ni/Au (20/100/25/50 nm) stack was lifted-off and subjected to rapid thermal annealing (RTA) at 850 °C in N_2 ambient for 30 s. Lastly, mesa isolation was achieved by Cl_2/BCl_3 etching.

Using this process flow, five rounds of process parameter optimization were conducted. The final parameters are presented in Table 2.2. The original RIE parameters, which are used as a starting point, are included for reference. In each round, these parameters (except pressure) were



Duration of etch (min.)	Type of Contact Obtained
0	Schottky
3	Schottky
5	Schottky
7	Schottky
8	Ohmic
9	Ohmic
10	Ohmic
11	Ohmic
12	Ohmic
13	Ohmic

Figure 2.16: Process development of the ICP-RIE selective etch (final round of optimization of recipe parameters, except for etch duration). (a) In the final round of optimization, with the other parmeters fixed, the duration of the etch was varied on various regions of Epi-2, and the ohmic contact (ohmic/Schottky) was characterized. (b) A representative double sweep profile showing ohmic behavior for contacts on Epi-2, after 12 min. of etch. (c) A representative double sweep profile showing ohmic behavior for contacts on Epi-3.

Table 2.2: Comparison of the parameters of the optimized ICP-RIE recipe and original RIE recipe for selective etch.

Parameter \ Tool	RIE Tool (Starting Point)	ICP-RIE Tool (Optimized Recipe)
Pressure (Pa)	5.2	5.2
ICP power (W)	90	120
Bias	120 V [1]	20 W
BCl_3/SF_6 flow (sccm)	16/32	42.5/7.5

[1] Approximate value of measured DC voltage.

varied, and different etch durations were tested in different regions of the same sample, as shown in Fig. 2.16(a). Epi-2 was used in the process development, because extensive characterization of its selective etch (Fig. 2.7(b) and Ref. [74]) was been conducted in earlier works. Finally, in Round 5, ohmic behavior was obtained in the contacts, after a certain etch duration. At short durations, the p-GaN was not completely removed, therefore the alloyed Ti/Al/Ni/Au contacts exhibited Schottky behavior. For an etch duration exceeding 8 min, the contacts exhibited ohmic behavior. This indicates that the top p-GaN has been sufficiently removed. A representative transfer length method (TLM) I-V curve for Epi-2 is shown in Fig. 2.16(b). Similar curves, but for Epi-3, are shown in Fig. 2.16(c). The I-V shows linear behavior near $V = 0$ V, and repeated double sweeps indicate negligible hysteresis within the sweep resolution.

Then, the newly developed ICP-RIE selective etch recipe was transferred to Epi-1 and Epi-3, which represent the GaN-CMOS platform and a structure with p-GaN resembling a commercial design, respectively. The best TLM results are reported in Fig. 2.17(a)–(b). For Epi-1, the best $R_c = 0.25$ Ω·mm ($R_{sh} = 343$ Ω/□) is obtained. For Epi-3, the best $R_c = 0.32$ Ω·mm (for $R_{sh} = 527$ Ω/□) is obtained. In particular, in the case of Epi-1, the excellent R_c combined with R_{sh} attests to the potential of the proposed ICP-RIE recipe.

Upon establishing the duration of etch needed for achieving ohmic behavior in the contacts, the impact of a higher duration etch was studied, as presented in 2.17(c)–(d). The proposed selective etch recipe gave ohmic contacts with Selective etch gave ohmic contacts with $R_c < 0.5$ Ω·mm and $R_{sh} = 300 \sim 450$ Ω/□ range. Therefore, the $14 \sim 18$ min. range would be suitable. The wide

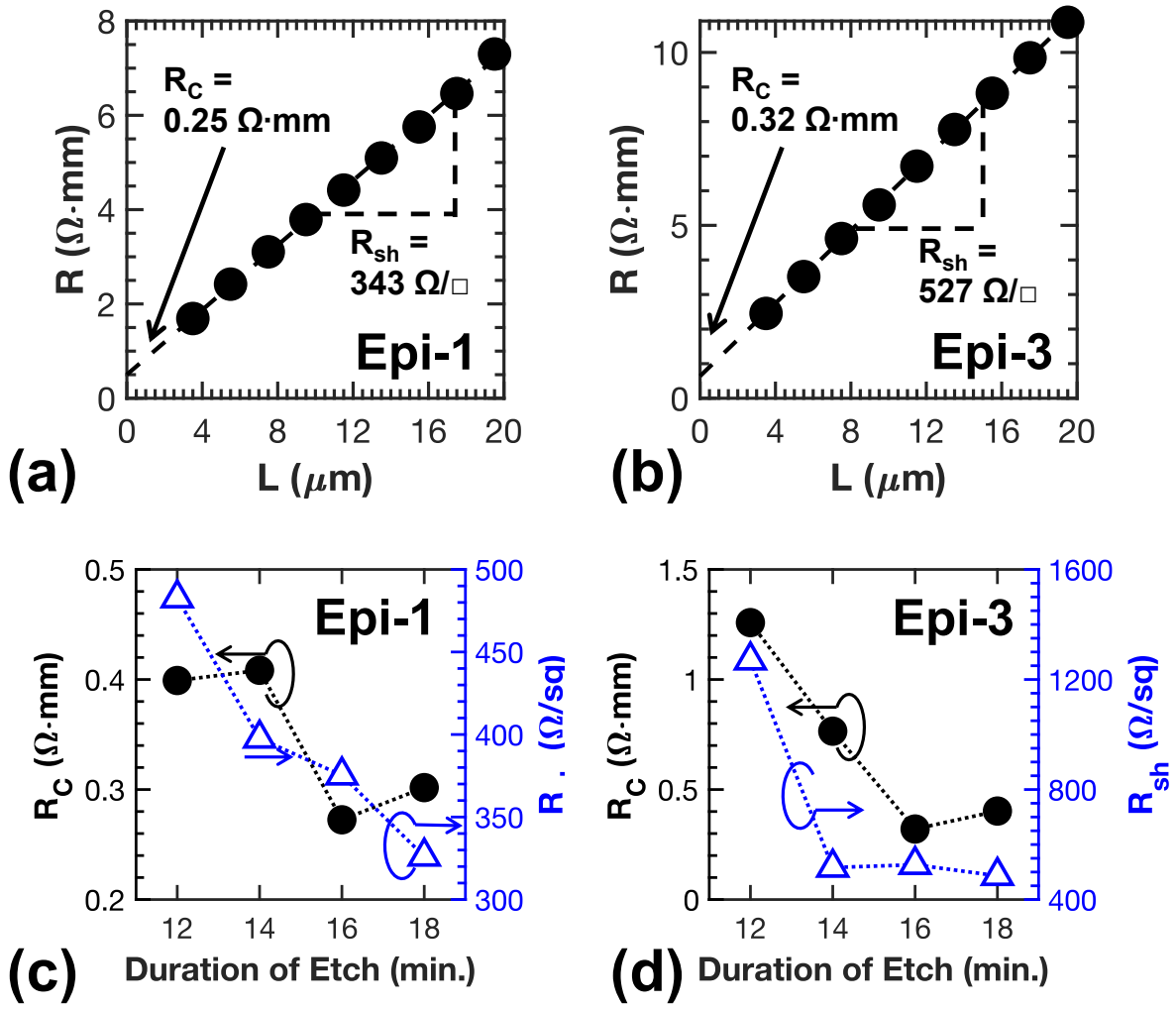


Figure 2.17: TLM measurement results of the ohmic contacts fabricated on AlGaN/GaN after ICP-RIE selective etch. (a)–(b) Best TLM results for Epi-1 and Epi-3, respectively. (c)–(d) Impact of duration of etch on R_c for Epi-1 and Epi-3, respectively.

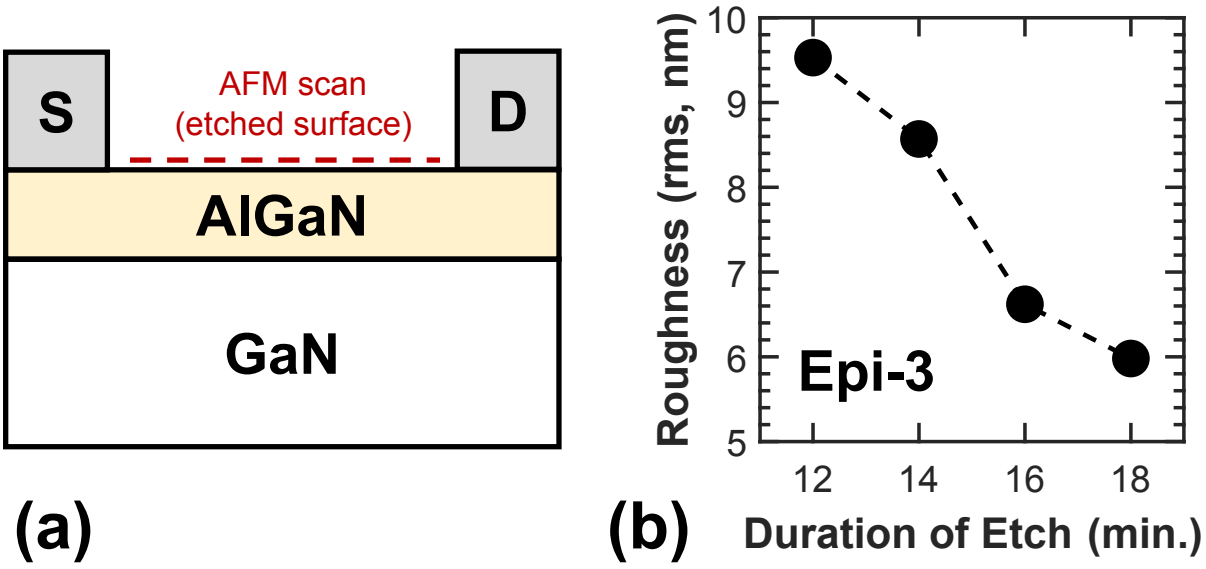


Figure 2.18: Surface morphology of the AlGaN surface after the ICP-RIE selective etch. (a) Indication of location of atomic force microscope (AFM) scan. (b) Impact of duration of etch on roughness for Epi-3.

range of etch duration ensures robustness of proposed recipe against variations of etch rate with time.

The samples were further characterized using an atomic force microscope (AFM) to study the surface morphology, as presented in Fig. 2.18. As the duration of etch increase, the surface roughness decreases. This is consistent with the theory that the p-GaN is entirely etched and the etch gradually stops on the AlGaN layer. It should be noted that, the roughness of 6 nm could be improved, possibly with a longer duration of etch, though the impact on the R_c needs to be taken into consideration (over-thinning of AlGaN would lead to increased sheet resistance in the access regions). Other methods for atomic-level treatment of the post-etch surface (after p-GaN etching) have been reported [110].

In summary, a recipe for selective etch of GaN (over AlGaN) was successfully developed using a new ICP-RIE tool. $R_c = 0.25$ Ω·mm (best result for Epi-1, GaN-CMOS platform) and $R_c = 0.32$ Ω·mm (best result for Epi-3) were obtained using conventional alloyed contacts. A wide process

window (ranging across > 4 min.) for duration of etch was observed. This work confirms that the proposed recipe is suitable in the future fabrication of HEMTs (n-FETs) on the GaN-CMOS platform.

2.7 Conclusion

Advanced scaling based on self-aligned features, as proposed in this work, offers a viable technology path for future high performance GaN complementary technology based on a MOCVD GaN-on-Si platform. The scaled p-FETs and n-FETs achieve competitive performance in their respective categories, and when taken together, deliver a leading GaN CT solution. An ICP-RIE selective etch was developed with excellent n-FET ohmic contacts obtained. This selective etch could be used in the future GaN-CMOS platform.

Further design innovation and engineering of the proposed technology would greatly benefit the eventual wafer-level heterogeneous integration of GaN CT (based on a Si substrate) with Si CMOS to achieve multi-functional chips [111].

Chapter 3

Si-CMOS-Compatible GaN p-FET

A major challenge to the commercialization of GaN-CMOS is Si-CMOS-compatibility (in other words, ensuring that GaN-CMOS is compatible with Si-CMOS foundries), without much sacrifice to the transistor performance. GaN p-FETs share many challenges in Si-CMOS-compatibility with GaN HEMTs (e.g. large-diameter wafers [45], contamination control of Ga [112]), where significant progress has been made. A unique challenge of p-FETs is that the reported high performance transistors rely on alloyed gold-based ohmic contacts (e.g. Ni/Au [71]), where Au facilitates the formation of a Au-Ga alloy (hence, inducing Ga vacancies) and achieves low resistivity in the ohmic stack [85]. Furthermore, long-term gold diffusion has been associated with the degradation of GaN ohmic contacts [113]. Some low resistance p-GaN contacts incorporate Mg (e.g. Mg/Ni/Au [105], Mg/Pt/Au [114]). Non-gold contacts in p-FETs include Ni/Ag on MOCVD p-GaN [107], and Pd/Ni on molecular beam epitaxy (MBE) p-InGaN/GaN/AlN-on-sapphire [115].

In spite of the recent progress in varieties of ohmic contacts for GaN p-FETs, from a commercialization perspective, the above-mentioned p-GaN ohmic schemes pose several problems: (1) Si-CMOS-incompatible metals (e.g. Ag, Mg, Pt, Au); (2) challenging integration in a transistor process (e.g. Mg); and (3) difficult MOCVD growth of p-InGaN with high Mg ionization ratio to give low-resistance contacts. Therefore, a Si-CMOS-compatible metallization scheme for MOCVD p-GaN remains a major bottleneck to achieving Si-CMOS compatiblility in GaN-CMOS.

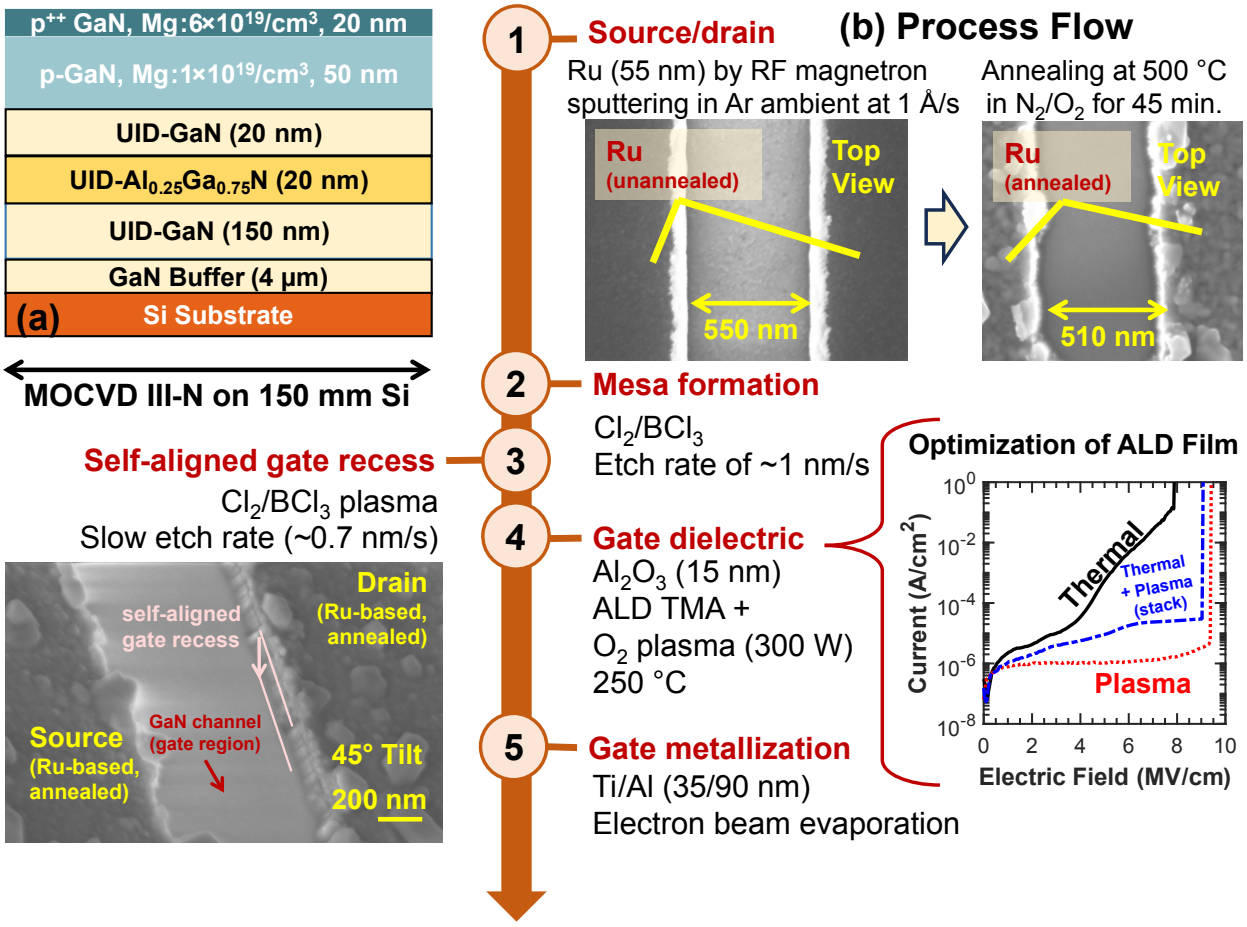


Figure 3.1: Process flow of Si-CMOS-compatible GaN p-FETs. (a) Starting epitaxial structure. (b) Process flow, consisting of 5 main stpes, namely (in sequence) source/drain, mesa formation, self-aligned gate recess, gate dielectric, and gate metallization.

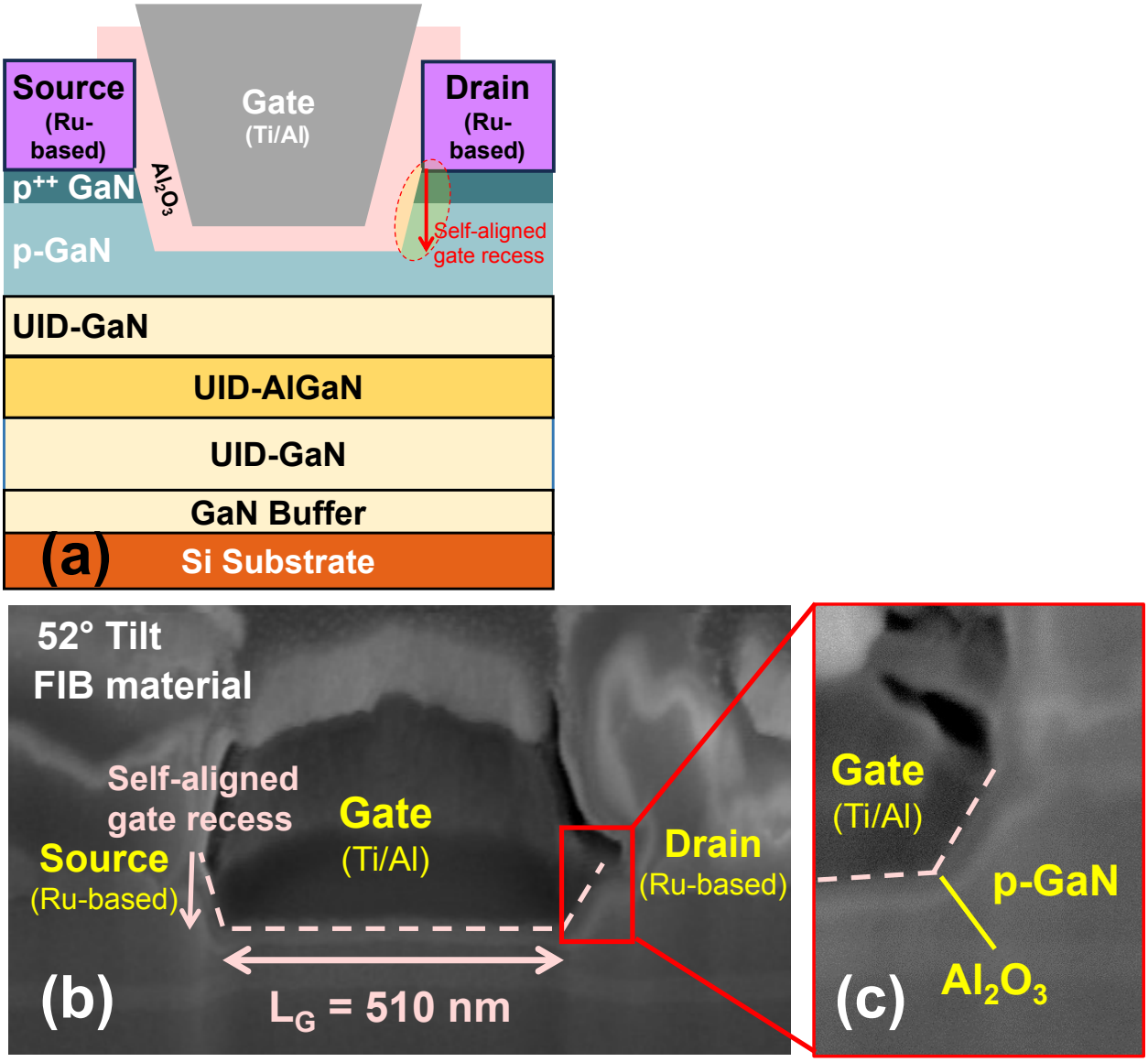


Figure 3.2: Si-CMOS-compatible GaN p-channel FETs with Ru-based S/D. (a) Schematic. (b) Cross-section (focused ion beam cut) of the fabricated transistor. (c) Zoom-in view of the gate region.

This chapter proposes the integration of Ruthenium (Ru)-based contacts into self-aligned-gate p-FETs based on a MOCVD GaN-on-Si platform. Ru is readily available in Si foundries for its use in interconnects and dynamic random-access memory (DRAM) [116], and has been explored as a Schottky gate in GaN HEMTs [117]. The proposed platform, in addition to being compatible with conventional Si fabs, exhibits promising properties for commercialization, namely: (1) scalable to wafer diameters beyond 200 mm [45]; (2) monolithic integration of p-FETs and n-FETs without costly regrowth steps [26]; (3) high transistor performance through aggressive scaling [71]. Furthermore, a novel self-aligned gate recess technology is demonstrated on the proposed p-FETs to achieve excellent E-mode transistors. The proposed transistors feature state-of-the-art performance among planar MOCVD III-N p-FETs.

3.1 Ru-Based Contacts and Their Integration in p-FET

As shown in Fig. 3.1(a), the epitaxial structure used in this work consists of p^{++}-GaN ([Mg]= 6×10^{19} cm^{-3}, 20 nm) / p-GaN ([Mg]= 1×10^{19} cm^{-3}, 50 nm) / UID-GaN (20 nm) / UID-$Al_xGa_{1-x}N$ (20 nm, $x = 0.25$) / UID-GaN buffer (UID: unintentionally doped), grown by MOCVD on a 150 mm Si substrate. 15 mm $\times$ 15 mm samples were used for the experiment.

3.1.1 Fabrication of p-FET with Ru-Based Contacts

The transistor fabrication [Fig. 3.1(b)] begins with the formation of source/drain (S/D) contacts by sputtering of Ru. 55 nm of Ru was sputtered from a high purity (99.95% Ru target) in Ar ambient. RF magnetron sputtering was conducted at a rate of 1 Å/s. A base pressure (without gas flow) of $< 4 \times 10^{-6}$ Torr (approximately the highest vacuum achievable by that particular sputtering tool) was ensured so as to obtain a high quality Ru film. Ru was patterned by a lift-off technique. Then, Ru was annealed at 500 °C in N_2/O_2 ambient in a furnace (annealing tube). The sample was loaded in the furnace at 250 °C, then the temperature was ramped up to 500 °C, stabilized for 10 min. (all in N_2 ambient), followed by flowing N_2/O_2 ambient in 1:2 ratio for 45 min. Then,

the furnace was cooled down for the removal of the sample. It could be seen from Fig. 3.1(b)(1) that, before the annealing, the freshly sputtered Ru showed fine grains. The annealed Ru surface roughened. Furthermore, the L_{SD} (distance between adjacent Ru contacts) was reduced slightly. Then, mesa isolation was performed using Cl_2/BCl_3. Even though the mesa and ohmic steps are interchangeable, the ohmic contact was chosen as the first step so as to maintain a "pristine p^{++}-GaN surface" for the formation of the best possible ohmic contact.

Then, the self-aligned gate recess (masked by the Ru-based S/D) was performed. This step was optimized for a relatively slow etch rate ($\sim$ 0.7 nm/s): (1) To reduce damage to the p-GaN in the gate region; (2) to protect Ru-based S/D (mask) from significant degradation. In previous works of the self-aligned gate recess [61], Ni (top layer in the Ni/Au/Ni S/D) was used as an etch mask against Cl-based plasma. In fact, Ni is also an excellent mask for high aspect ratio vertical fin etches [118, 119]. On the other hand, Ru may be etched in Cl_2/O_2 [120]. The gate recess etch was based on Cl_2/BCl_3 without any O_2, and done at a relatively slow GaN etch rate. Furthermore, the etch chamber was thoroughly cleaned to remove any residue of O_2. Fig. 3.1(b)(3) shows that, the gate recess is masked by the Ru-based S/D, and it etches into the GaN channel (gate region).

Lastly, the gate stack was formed. The gate dielectric is critical in MIS structures, especially in p-FETs where it serves as the potential barrier between a doped channel and the gate metal. There are previous examples of how poor gate dielectric leads to poor gate control and high gate leakage (low ON/OFF ratio) [71]. In this work, three films were deposited using the same plasma-enhanced atomic layer deposition (PEALD) tool, namely, thermal (TMA + H_2O, 15 nm), plasma (TMA + O_2 plasma, 15 nm), and a stack consisting of thermal (5 nm) and plasma (10 nm) (TMA: trimethylaluminium). In the configuration of the PEALD tool, the O_2 plasma is "remote plasma," where plasma is remotely generated, then flown into the chamber, as opposed to "direct plasma." Therefore, the surface is not expected to be significantly affected by O_2 plasma. In fact, direct O_2 plasma treatment (e.g. in an RIE tool) was reported to serve as an effective surface treatment and result in E-mode characteristics [121]. In order to quantify the characteristics of the ALD films, metal-insulator-metal (MIM) capacitor structures are fabricated immediately before the actual run.

Two main aspects of the characteristics are examined, namely, the leakage at lower electric field, and the breakdown voltage (which is important because the breakdown of self-aligned p-FETs is limited by the gate dielectric). Among the three films, the plasma ALD film shows the lowest gate leakage (consistent leakage in 1 $\mu A/cm^2$ range for < 8 MV/cm), before breaking down at 9.5 MV/cm. Therefore, plasma ALD (250 W O_2 plasma) was chosen for the actual deposition of the gate dielectric in the p-FET. Other precautions for the ALD include, measuring the uniformity of the ALD across the entire 200 mm chamber. In this work, the uniformity was < 1 nm which is considered within the error margin of the ellipsometer and Cauchy model.

Lastly, the gate metallization was achieved with the electron beam evaporation of Ti/Al (35/90 nm). The schematic of the completed transistor is shown in Fig. 3.2. The SEM (FIB cut) of a representative transistor is in Fig. 3.2(b). The zoom-in view of the gate stack (Fig. 3.2(c)) reveals that, (1) the etch sidewall profile is sloped (not fully vertical), which is the result of the use of a lower power plasma etch; (2) a conformal Al_2O_3 layer is deposited in the gate recessed region, and the gate metal filled up the entire gate recessed region (on top of the gate dielectric). In this work, most etch depths are approximately $50 \sim 70$ nm, and compared to $L_G = 510$ nm, the aspect ratio of the gate recessed region makes it easy for the metal (electron beam evaporation) to conformally fill up the entire region. In the case of ultra-scaled channel lengths $L_G < 100$ nm, considering that there is also S/D metal, the aspect ratio of the "trench" is $> 1:1$. While ALD could easily fill up such trenches, sputtering could be adopted to achieve conformal deposition in the trench. The details of the process flow (baseline p-FET and formation of Ru-based S/D contacts) are available in Appendix A.

3.1.2 Material and Electrical Characterization of Ru-Based Contacts

The Ru/p-GaN interface (after annealing at 500 °C) was characterized using high resolution (HR) transmission electron microscopy (TEM). According to the HR-TEM image [Fig. 3.3(a)–(b)], A high-quality interface was obtained. Furthermore, selected area diffraction pattern (SADP) technique was used to characterize the Ru/p-GaN interface, which is of central interest to this work.

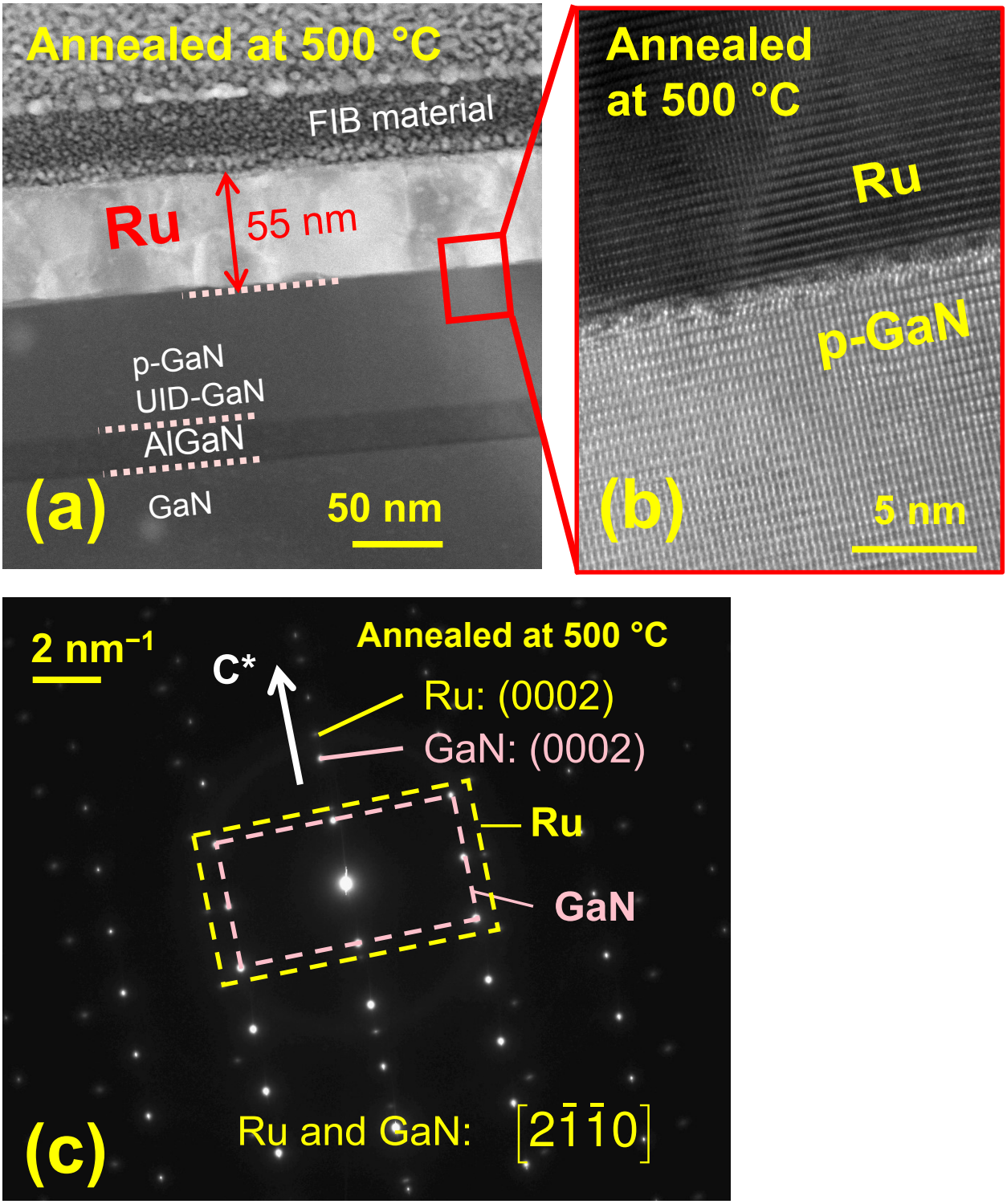


Figure 3.3: Transmission electron microscopy (TEM) of the Ru-based S/D contacts. (a)–(b) Ru on p-GaN epitaxy; (c) selected area diffraction pattern (SADP) of Ru/p-GaN interface. In (a)–(c), Ru was annealed at 500 °C.

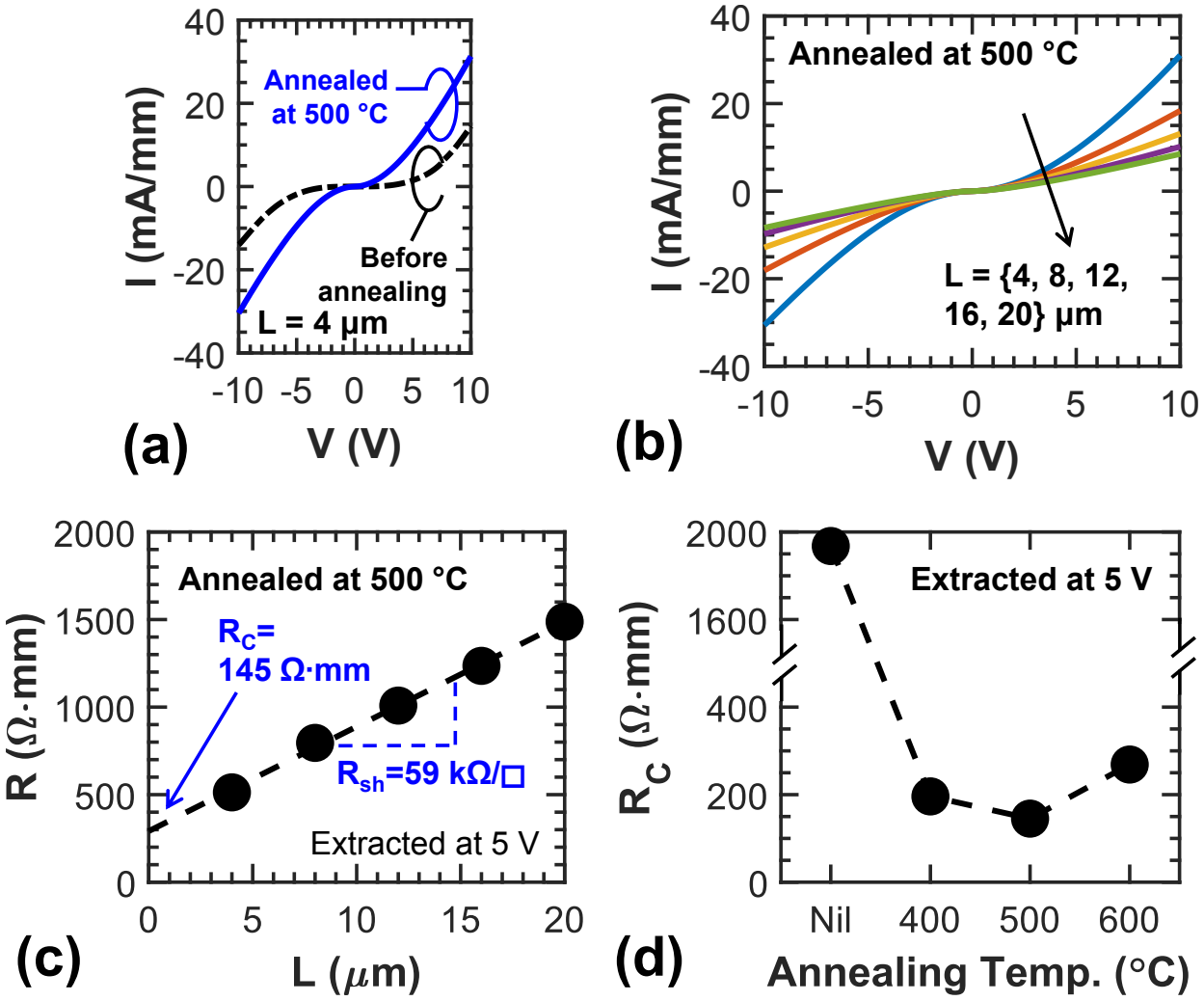


Figure 3.4: Electrical characterization of TLMs of Ru-based contacts: (a) Impact of annealing; (b) I-V curves of TLM structures; (c) TLM fitting; (d) Optimization of annealing temperature.

As shown in Fig. 3.3(c), Ru is in single crystalline (hexagonal) form and is well-aligned with the hexagonal GaN crystal.

The impact of the annealing conditions on the electrical performance of Ru-based S/D contacts was studied through the transmission length method (TLM). As shown in Fig. 3.4(a), after annealing, the current approximately doubled and the Schottky turn-on behavior was significantly reduced. The TLM method was used to extract R_c, [Fig. 3.4(b)–(c)]. Given the Schottky nature of the proposed ohmic contacts (and most ohmic contacts used for p-FETs), a constant voltage method (at $V = 5$ V) was used to extract the value of resistance, or $R = 5\text{ V}/I(V = 5\text{ V})$. Several different annealing temperatures were experimented (with other annealing conditions kept the

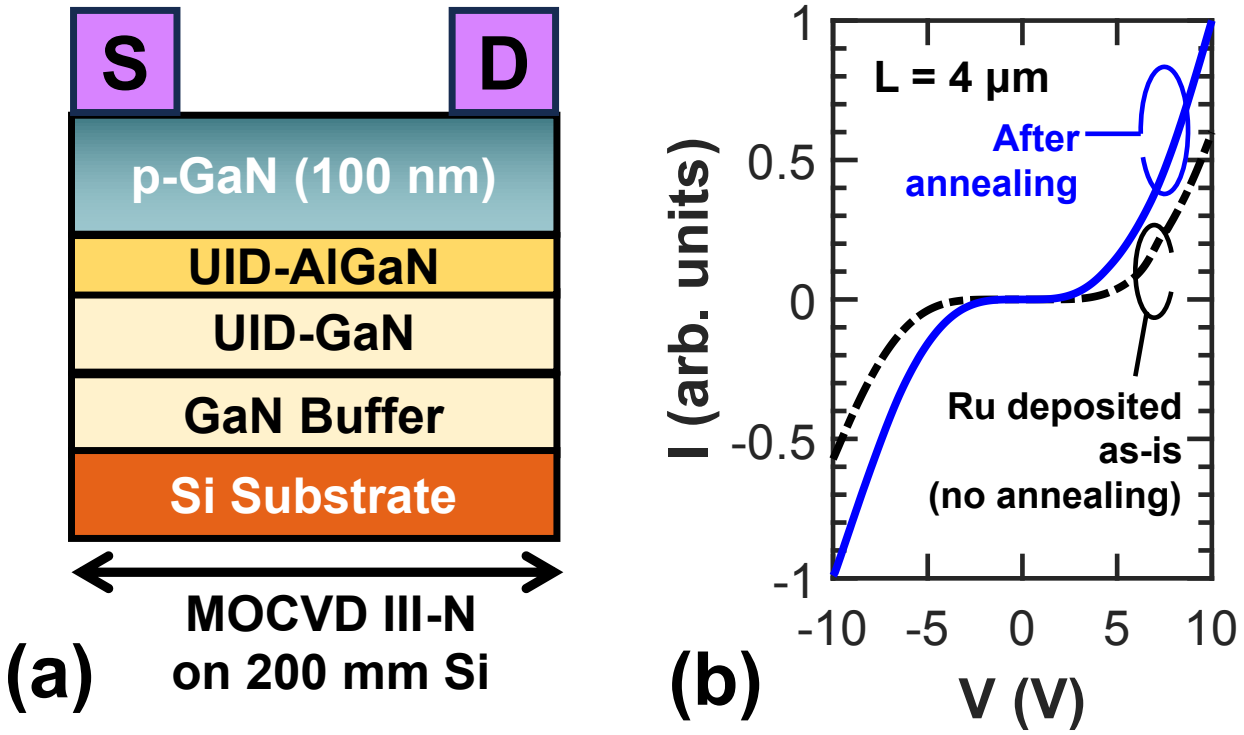


Figure 3.5: Ru-based S/D contacts on conventional p-GaN wafer. (a) Epitaxial structure of conventional p-GaN wafer with 100 nm of graded p-GaN. (b) TLM measurement before and after annealing (500 °C).

same). According to Fig. 3.4(d), 500 °C was found to be the optimal annealing temperature.

While most this work was conducted on Epi-1 (GaN-CMOS platform), the feasibility of the proposed Ru-based contact on a conventional p-GaN epitaxy was also explored. In this conventional p-GaN epitaxy [Fig. 3.5(a)], there is no custom-designed p^{++} layer at the top of the epitaxy, instead the Mg doping follows a natural linearly increasing profile (from the top of the AlGaN) due to doping delay and memory effect. The thickness of the p-GaN is 100 nm which is similar to commercially used wafers. The TLM characteristics are shown in Fig. 3.5(b), where annealing improved the current density. However, comparing between Fig. 3.5(b) (conventional epitaxy) and Fig. 3.4(a) (GaN-CMOS epitaxy), it is observed that a slightly higher turn-on voltage is obtained in the conventional epitaxy, due to the lower p-GaN doping at the surface. Nevertheless, this study

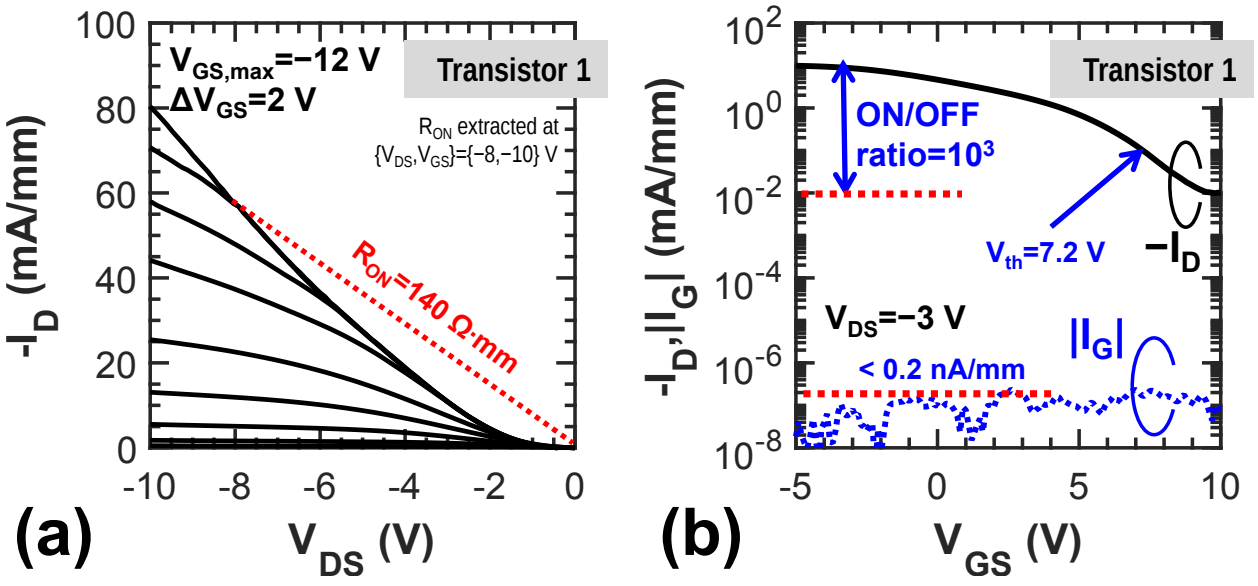


Figure 3.6: Performance of a p-FET with Ru-based S/D ("Transistor 1", $L_G = 510$ nm, $W = 20$ µm). (a) Output characteristics. (b) Transfer characteristics.

establishes the basis for the future transfer of the proposed Si-CMOS-compatible contacts (and p-FETs) to commercially available p-GaN power platforms.

3.2 Transistor Performance

The performance of the p-FET with the best overall characteristics ("Transistor 1"), $L_G = 510$ nm (self-aligned to L_{SD}), is presented in Fig. 3.6. This planar transistor exhibits $I_{D,max} = -80.3$ mA/mm, $R_{ON} = 140$ Ω·mm (extracted at $\{V_{DS}, V_{GS}\} = \{-8, -10\}$ V) [Fig. 3.6(a)]. D-mode operation ($V_{th} = 7$ V, extracted at $I_D = -0.1$ mA/mm) was obtained [Fig. 3.6(b)]. The ON-OFF ratio (10^3) is limited by the source-drain leakage current, which indicates the presence of a substantial conductive GaN channel underneath the gate [70].

For p-FETs, careful calibration of the recess depth is required to achieving E-mode operation [72], which is desired in power and digital ICs. The gate recess also impacts other transistor characteristics, as will be explained in Chapter 4.1. A schematic illustrating self-aligned gate recess in the p-FET with Ru-based S/D is available in Fig. 3.7, showing that in this ohmic-first process, the Ru-based S/D ohmic acts as the mask for the self-aligned gate recess.

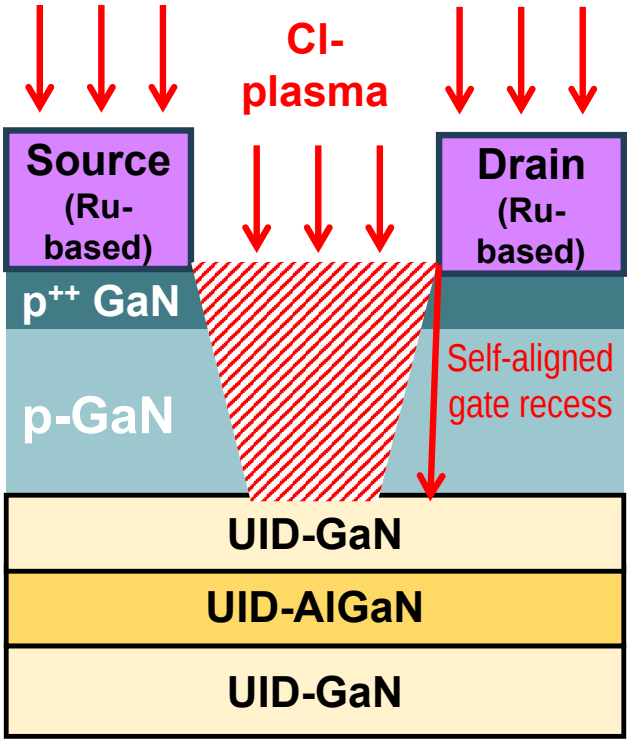


Figure 3.7: Schematic illustrating self-aligned gate recess in the p-FET with Ru-based S/D.

3.2.1 E-Mode p-FET using Novel Technology for Self-Aligned Gate Recess

Here, a novel technology for self-aligned gate recess is proposed for better control of the recess depth, therefore optimization of $I_{D,max}$, V_{th} and $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$. Before this work, for the gate recess step, a single time-controlled etch run of >70 nm was conducted. However, there are several limitations, most notably, that accurate (and repeatable) relationships between etch depth and etch duration, as well as $I_{D,max}$ and etch depth, need to be known *a priori*. Ultimately, it is the transistor characteristics that are the most important, rather than absolute values of recess depth. The problems are often compounded by unstable etch rates (e.g. contamination in the chamber, or drift in conditions over time), and difference in the p-GaN uniformity (thickness and doping profile) across the sample. While the detailed characterization of these relationships would improve on the situation, this work proposes a novel gate recess technology which takes advantage of the self-aligned gate architecture (with ohmic-first process) to achieve a better controlled gate recess.

Instead of a single time-controlled etch run, a multi-step gate recess was used [Fig. 3.8(a)] with

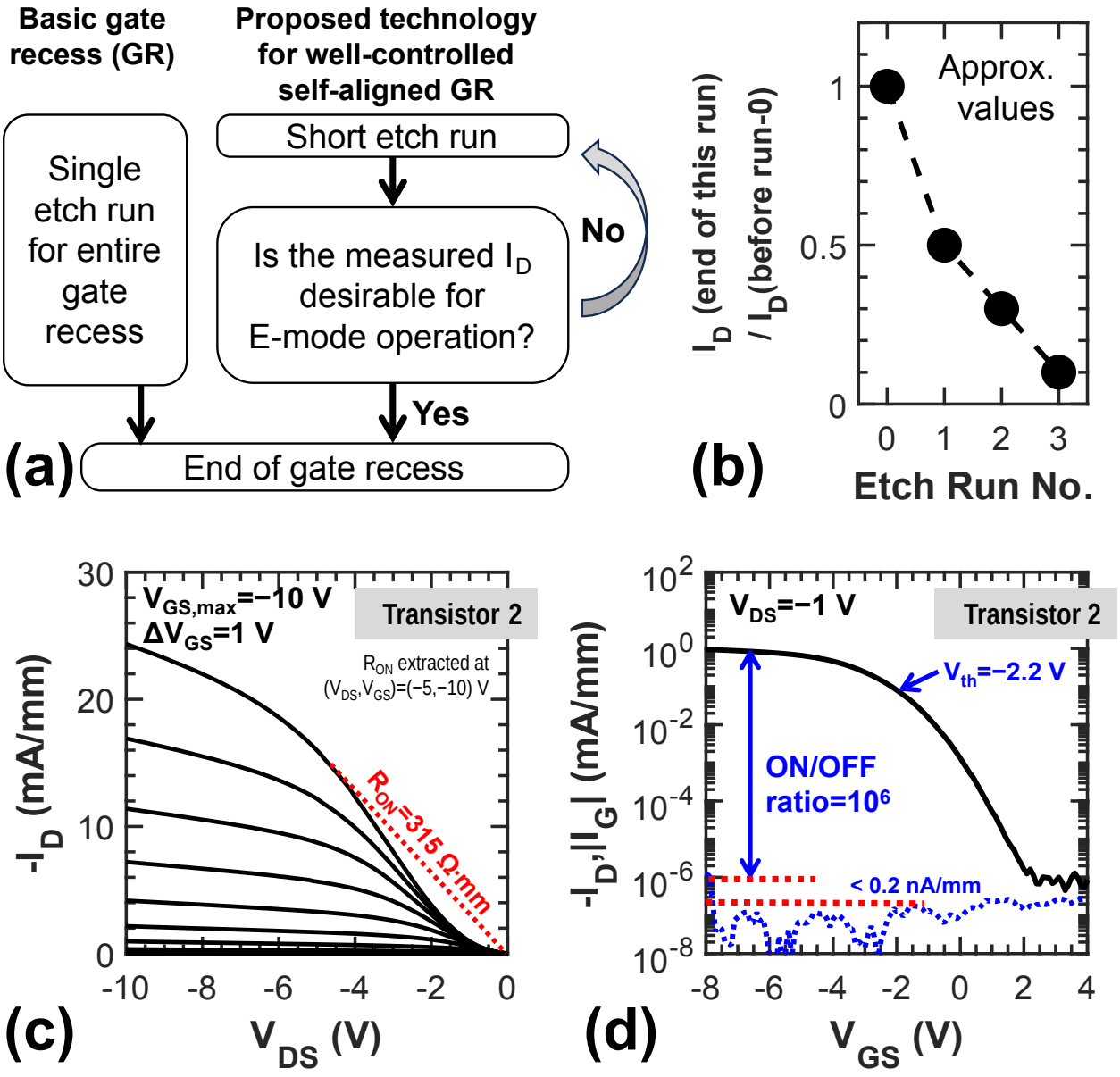


Figure 3.8: Achieving E-mode operation through a novel technology for gate recess. (a) Flow chart. (b) Electrical measurement which facilitates the proposed technology. Values are approximate but representative of a typical etch process. Performance of a transistor ("Transistor 2", $L_G = 510$ nm, $W = 20$ µm) fabricated using this technology: (c) Output characteristics; (d) Transfer characteristics.

a smaller recess depth per run ($\sim$ 20 nm). I_D is monitored after each etch and used to determine the additional recess in subsequent cycle(s) [Fig. 3.8(b)]. This method is made possible because of the self-aligned gate recess architecture and the excellent robustness of Ru-based S/D to the gate recess etch.

By leveraging the proposed gate recess technology, the best E-mode transistor ("Transistor 2", $L_G = 510$ nm) achieved $V_{th} = -2.2$ V (extracted at $I_D = -0.1$ mA/mm), $I_{D,max} = -24.3$ mA/mm, $R_{\mathrm{ON}} = 315$ Ω·mm (extracted at $\{V_{DS}, V_{GS}\} = \{-5, -10\}$ V), $I_{\mathrm{ON}}/I_{\mathrm{OFF}} = 10^6$ [Fig. 3.8(c)–(d)]. The strong E-mode operation and good current saturation makes it desirable for power and mixed-signal GaN-CMOS circuits. The breakdown voltage is $\sim$ 17 V and is limited by the destructive breakdown of the gate dielectric between the gate and drain. The breakdown field of the Al_2O_3 film was determined to be 8.7 MV/cm from measurements of metal-Al_2O_3-metal capacitors. In Transistors 1 and 2, a low gate leakage of < 0.2 nA/mm was obtained, which attests to the excellent quality of the gate dielectric. The transistors exhibit slight Schottky turn-on behavior, commonly observed in many p-FETs, with likely reasons being the S/D contacts and p-GaN/UID-GaN Schottky barrier [122].

3.3 Benchmarking

The benchmarking of this work is presented in Fig. 3.9. In this work, a D-mode p-FET (Transistor 1) and an E-mode p-FET (Transistor 2) were demonstrated. Here, it should be highlighted that, the D-mode and E-mode p-FETs have different implications for the domain of GaN p-FET and GaN-CMOS. From an application-driven perspective, the E-mode p-FET is meaningful for power and digital ICs, where they are monolithically integrated with the E-mode n-FET. On the other hand, the D-mode p-FET serves as the "golden standard" for assessing the drive current handling capability ($I_{D,max}$). Such an assessment is relevant for the particular epitaxial structure on which the particular transistor architecture is fabricated, so different data points represent the variations in *(both)* epitaxial structures *and* transistor architectures. This is considering that, $I_{D,max}$ of D-mode

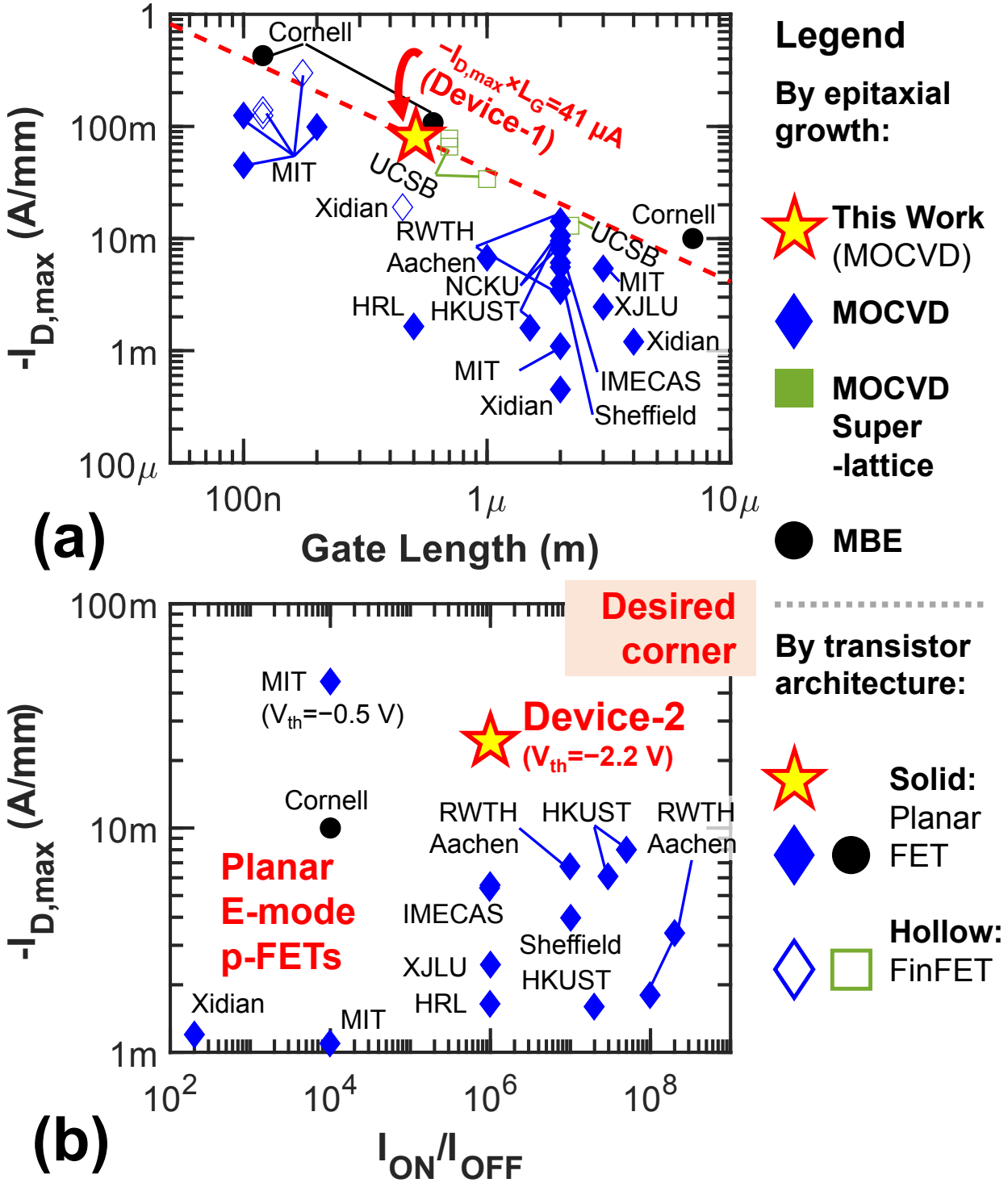


Figure 3.9: Benchmarking of this work (Si-CMOS-Compatible p-FETs) with reported III-N p-FETs. (a) $-I_{D,max}$ *vs.* L_G, which reflects the potential of the transistor for aggressive scaling. This work (Transistor 1) achieves a record $-I_{D,max} \times L_G$ among planar MOCVD p-FETs. (b) $-I_{D,max}$ *vs.* I_{ON}/I_{OFF} of planar E-mode transistors. This work (Transistor 2) features a desired combination of $-I_{D,max}$ and I_{ON}/I_{OFF}, while maintaining strong E-mode. The results represent the first demonstration of GaN p-FETs with Si-CMOS-compatible metallization on GaN-on-Si.

p-FETs tend to be higher than that of E-mode p-FETs.

Therefore, it is advocated that, the focus of benchmarking in D-mode p-FETs should be on the drive current. It is also acknowledged that a basic parameter that strongly impacts the drive current is the gate length L_G, which creates a trade-off between $I_{D,max}$ and L_G. This work (Transistor 1) achieves $-I_{D,max} \times L_G = 41$ μA, which is a record value for planar MOCVD III-N p-FETs [Fig. 3.9(a)].

Furthermore, E-mode operation is critical for power and mixed-signal applications, so the trade-off between the ON and OFF-state characteristics should be examined. A commonly used benchmark for III-N p-FETs is $I_{D,max}$ *vs.* I_{ON}/I_{OFF}, which represent the ON and OFF-state characteristics, respectively. Among planar E-mode p-FETs, this work (Transistor 2) features a desired combination of $-I_{D,max}$ and I_{ON}/I_{OFF}, while maintaining strong E-mode ($V_{th} = -2.2$ V) [Fig. 3.9(b)]. To the best of the author's knowledge, the results represent the first demonstration of p-FETs with Si-CMOS-compatible metallization based on a GaN-on-Si platform. Furthermore, the reported transistors exhibit good scalability (thanks to large diameter GaN-on-Si wafers), Si-CMOS-compatibility, and easy integration with GaN n-FETs [72].

3.4 Conclusion

This work lays the foundation for Si-CMOS-compatibility in GaN p-FETs using Ru-based ohmic contacts on a scalable MOCVD GaN-on-Si substrate. The best transistor ($I_{D,max} = -80.3$ mA/mm, $R_{ON} = 140$ Ω·mm) advances the state-of-the-art $-I_{D,max} \times L_G$ of planar MOCVD III-N p-FETs. The reported E-mode p-FET, realized using a novel gate recess technology, exhibits excellent performance ($I_{D,max} = -24$ mA/mm, $I_{ON}/I_{OFF} = 10^6$, $V_{th} = -2.2$ V) among E-mode planar III-N p-FETs. The proposed Si-CMOS-compatible GaN p-FETs are therefore an important step towards the realization of Si-CMOS-compatible GaN-CMOS and the heterogeneous integration of GaN-CMOS on a Si-CMOS platform.

Chapter 4

Unique Design Space of GaN p-FETs

The materials in this chapter are partially based on the following publication.
Q. Xie *et al.*, "Highly Scaled GaN Complementary Technology on a Silicon Substrate," *IEEE Transactions on Electron Devices*, vol. 70, no. 4, pp. 2121–2128, Apr. 2023. [72]

Over the years, there has been significant advancement in MOCVD GaN p-FET performance, primarily through a combination of device structure innovation and process optimization. Given that GaN p-FET is a new and emerging area of research, currently the research has focused on proof-of-concept demonstrations of transistors with novel designs (material and device), optimized process flow or characterization. While the proof-of-concept demonstrations indicate promising performance, it is equally important to conduct a deep analysis of the unique characteristics of the p-FETs. Furthermore, in the longer term, such deeper understanding in the device characteristics would also deepen the understanding of the design space of the devices. For example, some studies have focused on analyzing the interface charge in GaN p-FETs, both in the oxide/p-GaN interface (for metal-insulator-semiconductor (MIS) structures) as well as the metal/p-GaN interface (for Schottky gate) [88, 123].

If one decomposes the p-FET (from a device structure point-of-view), there are several features (for a planar transistor), including the S/D ohmic contacts, the gate recess, and the gate stack. For

the p-FETs of this work, a glimpse of the optimization of (Ru-based) S/D ohmic contacts was reported in Chapter 3.1, while the optimized fabrication (and its issues) of the gate stack was discussed in Chapter 2.4. Therefore, this chapter focuses on the gate recess, which is a unique feature of p-FETs typically not present in HEMTs (or even if present, gate recess in HEMTs is typically shallow, < 20 nm).

4.1 Impact of Gate Recess on Design Space

In the case of the Ga-polar HEMT, the channel is close to the surface (only separated by a thin barrier). However, in the case of most p-FETs of various epitaxial structures, the p-channel is "buried" inside the epitaxial structure. The p-channel (2DHG) is typically present at a GaN/AlGaN (Ga-polar) heterostructure, and a sufficiently thick GaN (often p-GaN) is required to ensure high 2DHG charge density. Therefore, a gate recess etch is required to allow the gate metal to approach the buried channel. Note that, (1) for the p-FET to adopt a similar device structure as the Ga-polar HEMT, a N-polar AlGaN/GaN heterostructure would be required, though issues such as forming good ohmic contact would have to be resolved. (2) while some n-FETs (HEMTs) use gate recess (recess of the polarization-inducing barrier), the recess is typically shallow (< 20 nm), but in the case of p-FETs of this work, a deep gate recess up to 70 nm may be used.

The impact of gate recess is particularly important for most MOCVD p-FETs which feature p-GaN/UID-GaN (optional)/AlGaN, because of the existence of a doped bulk channel. Gate recess has been identified as an important design parameter since the early days, with reports of the impact of gate recess depth (in the implementation, different etch durations for a time-controlled etch) on the output characteristics of the p-FET, which illustrates the trade-off between the maximum current density and the ON-OFF ratio [69, 70]. In the second generation of the self-aligned p-FET [70], it was proposed that, the shallower gate recess allowed for the preservation of the bulk channel, therefore increasing the current density. However, there lacks direct verification or further substantiation of the impact of gate recess.

Proof-of-concept TCAD simulations are immensely valuable in early-stage research to explore novel device concepts, like in the case of p-FETs [124–126]. They are also valuable for exploring the design space of these novel transistors [127]. In the future, if GaN p-FETs were to be adopted for industrial R&D or even production, extensive TCAD would be required for the design technology co-optimization (DTCO) of GaN p-FET and GaN-CMOS. However, to the best of the author's knowledge, the vast majority of the p-FETs simulations are of the nature of "performance projections" and "exploration of design space" (without specific references to experimental results). However, reports of the TCAD of p-FETs to explain experimentally observed phenomena are scant, let alone TCAD results which are being verified by other (independent) experiments.

In the case of the impact of gate recess, TCAD simulation would be valuable to understand the mechanisms of charge accumulation/depletion in the device structure. More importantly, the transfer characteristics also deserve examination, and through TCAD simulation (and experimental measurements), the "double g_m peak" behavior is revealed and explained.

4.1.1 TCAD Simulation Study of Gate Recess

In order to study the "double turn-on" phenomenon from a device mechanism aspect, TCAD simulation of a two-dimensional TCAD structure (considering a planar structure p-FET, Fig. 4.1(a)) was conducted using Silvaco ATLAS.

4.1.2 Setup of TCAD Simulation

In order to isolate the effect of gate recess, the most basic p-FET structure was used, similar to that of [95]. A non-self-aligned p-FET (gate recess is not self-aligned to the S/D) structure and long channel dimensions ($L_{GS} = L_G = L_{GD} = 2$ µm) were used. (Note that L_G refers to the length of the gate foot (bottom of the recessed region). These parameters ensure that, the so-called "gradual channel approximation" could be applied in these p-FETs. In particular, the electric field in the depth direction (impacted by gate recess depth) should be independent of the electric field in the length direction. Note that the "depth" and "length" directions refer to the y- and x-directions

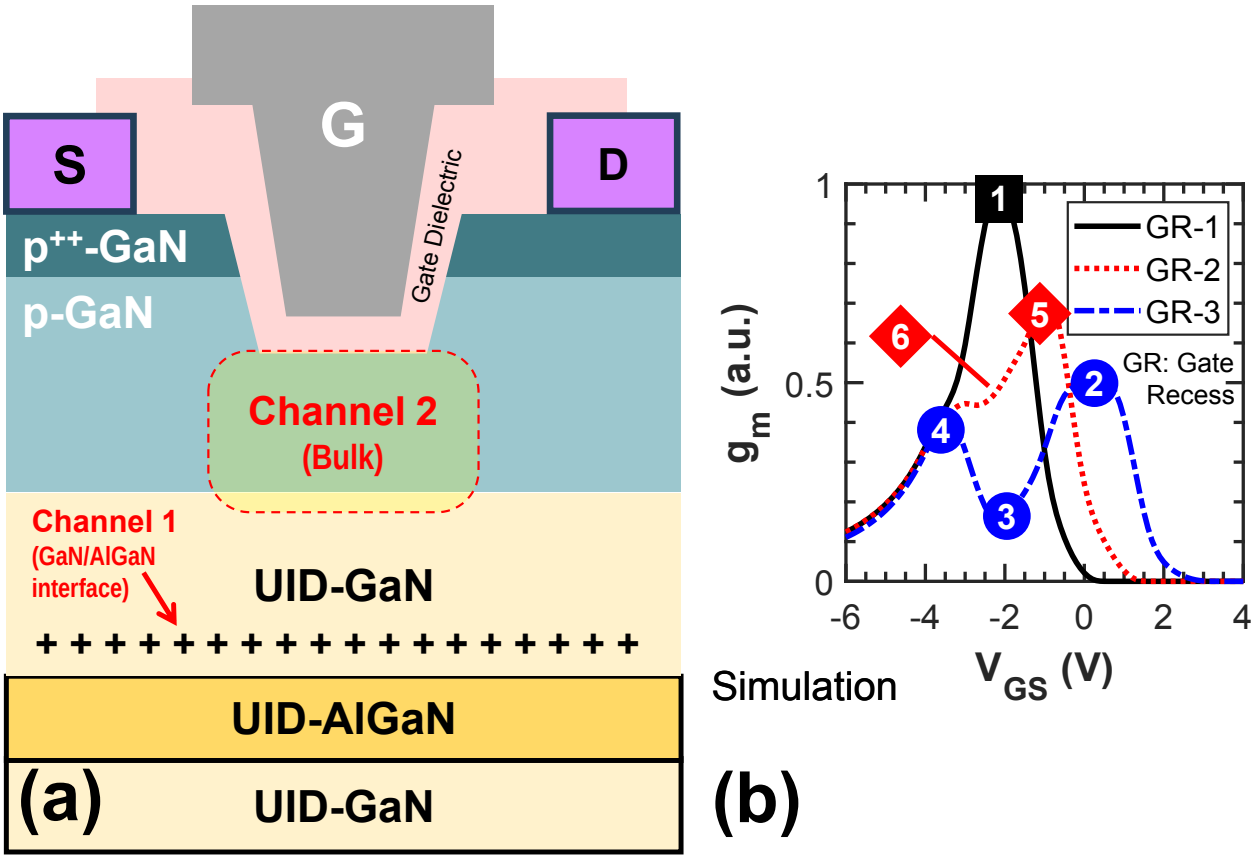


Figure 4.1: Unique g_m characteristics of p-FETs with dependency on the gate recess depth. (a) Schematic of device structure, showing the two channels, Channel 1 (GaN/AlGaN interface) and Channel 2 (Bulk GaN). (b) g_m characteristics as a function of gate recess depth (Depth: GR-$1 > 2 > 3$), simulated using Silvaco TCAD.

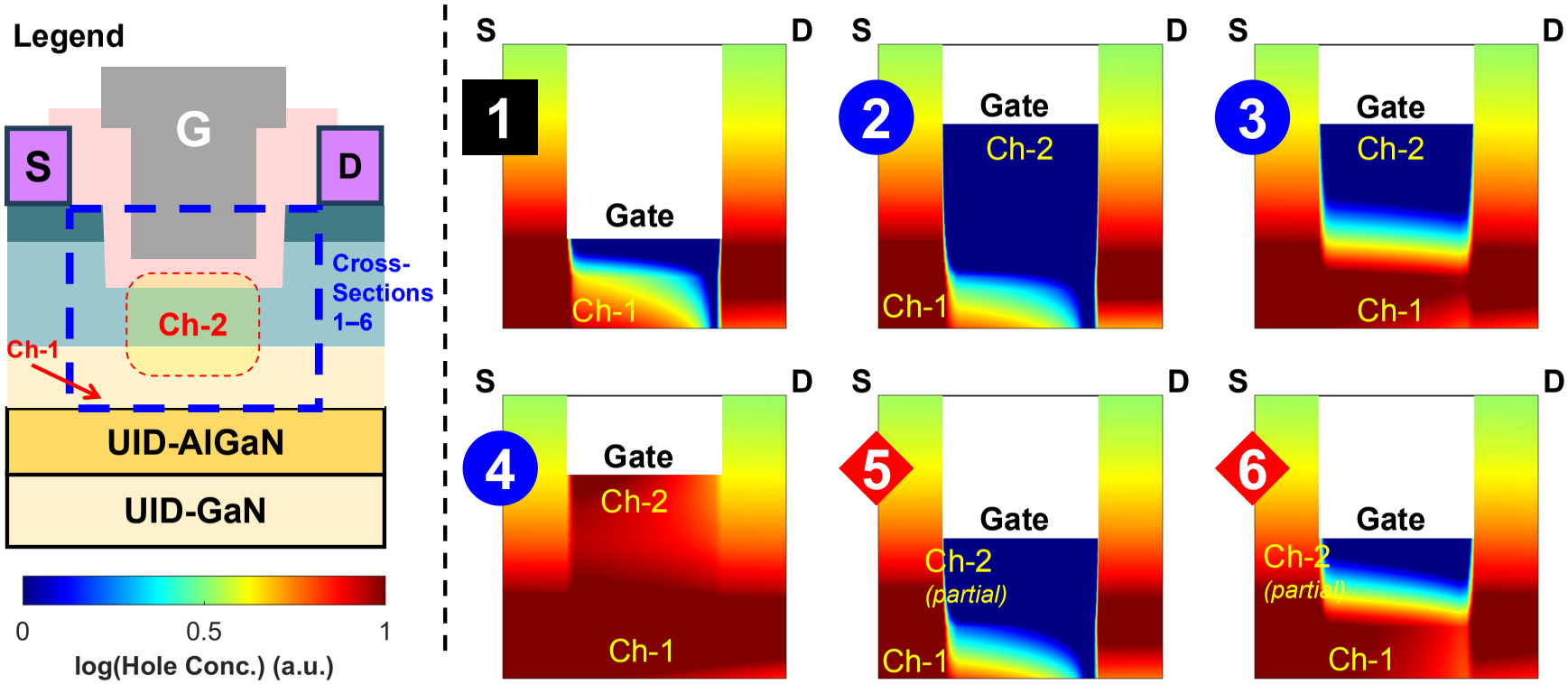


Figure 4.2: TCAD simulation of p-FETs to reveal the double g_m peak characteristics. The number labels in the sub-fugures correspond to the depth of gate recess (GR-{1,2,3}) and bias conditions (V_{GS}, V_{DS}), as shown in Fig. 4.1(b). The position of the two channels, Ch-1 and Ch-2, are labelled (unless absent). The extent of the cross-section is shown in the legend.

in the convention of Si-MOSFET, respectively. In terms of the p-doping, to simulate the doping delay and memory effect, as well as back-diffusion (out-diffusion) of Mg into the UID-GaN, a two-step doping profile in the GaN (above AlGaN) was assumed at 2×10^{19} cm^{-3} (top 50 nm, closer to surface) and 5×10^{18} cm^{-3} (bottom 40 nm, closer to AlGaN). Incomplete ionization ($\Delta E_A = 0.24$ eV) was assumed. An Al_2O_3 gate dielectric, a common choice for p-FETs, was used in the simulation.

A simplified mobility model was used, given that, this simulation is largely qualitative, and the transfer characteristics at lateral fields ($V_{DS} = 1$ V) is expected to be reflected in the simulation with little effect from the higher field mobility. The Caughey-Thomas model was used, with a fixed low-field mobility of 20 cm^2/V$\cdot$s (independent of doping concentration etc.). The details are available in the simulation code provided in Appendix B.

Three gate recess (GR) depths were chosen (labelled as GR-{1,2,3}), with GR-1 being the deepest gate recess, and GR-3 being the shallowest gate recess. It should be noted that, "gate recess depth" is the commonly used concept from a fabrication point of view (because of the characterization of the etch depth after the gate recess). On the other hand, it might be more intuitive from a device structure point of view to think of the thickness of p-GaN/UID-GaN (above AlGaN) remaining. Therefore, the deepest gate recess (GR-1) corresponds to the least thickness of GaN (above AGaN) remaining, and *vice versa*.

4.1.3 Simulation Results and Discussion

For the three p-FETs with different gate recess depths, a qualitative difference in g_m profiles was observed, as presented in Fig. 4.1(b). For a visualization of the electrical characteristics, the device cross-sections showing the local hole concentrations are included in Fig. 4.2.

In the case of GR-1, which is commonly featured in early demonstrations of GaN-on-Si p-FETs [95], a single g_m peak (bias point 1) was observed, which corresponds to the accumulation of the p-channel near the p-GaN/AlGaN interface.

Next, the case of GR-3, which corresponds to shallow gate recess (more p-GaN remaining),

is examined. A "g_m double peak" is observed. The first sub-channel (near the p-GaN/AlGaN interface) is activated at bias point 2 and its full accumulation is completed by bias point 3. Then, the activation of the second sub-channel (bulk p-channel underneath the gate metal) occurs at bias point 4.

Lastly, the case of GR-2 (gate recess depth in between GR-1 and GR-3) is examined. Similar to the case of GR-3, at bias point 5, the first sub-channel is activated. Then, at bias point 6, the theoretical peak contributed by the second sub-channel is less obvious. Therefore, this accumulation effect shows up as a kink in the g_m curve instead of a discrete peak. The phenomenon of GR-2 may be understood from two perspectives, (1) due to the limited amount of p-GaN remaining, the two sub-channels are not so distinct but are effectively fused into a single channel; (2) the theoretical g_m peaks contributed by the two sub-channels (as if they could be differentiated) are too close to each other (in terms of V_{GS}). In all the transistors, at high gate overdrive, all of the channels have been turned on, or that hole accumulation has occurred in the channels. This proof-of-concept simulation illustrates the impact of the sub-channels (whose existence is dependent on the recess depth) on the transfer characteristics of the p-FET.

The above simulation also supports the observation in earlier works that the maximum current density $I_{D,max}$ drops, but the ON/OFF ratio increases and the current saturation improves with increasing gate recess (less p-GaN remaining) [69, 70]. The reduction in $I_{D,max}$ is attributed to the reduction in total charge density (due to less bulk channel remaining). The improvement in ON/OFF ratio is attributed to the gate being closer to the entire channel, therefore the gate is able to exert greater electrostatic control over the channel. The improvement in current saturation is attributed to the better carrier confinement (in the depth direction), therefore, easier to achieve channel pinch-off which is necessary for current saturation (mobility-limited regime).

The experiment and simulation confirm the significance of the gate recess depth (as a key design parameter) in transistor performance, in terms of $I_{D,max}$, R_{ON} and transfer characteristics. This phenomenon is unique to the p-FET (as opposed to HEMTs) due to the design of the epitaxial structure (p-GaN/AlGaN/GaN) and transistor structure (gate recessed MISFET). The formation of

the p-channel at and surrounding the p-GaN/AlGaN interface is made possible by a highly p-doped material (p-GaN). The p-channel in the epitaxial structure is buried and therefore a simple top gate is not sufficient to exert electrostatic control over the entire channel. A recessed gate structure, while adding design flexibility to p-FETs, require special consideration in the design (recess depth and profile) and fabrication (e.g. reducing etch-induced damage [65, 70]).

4.1.4 Experimental Verification of TCAD Predictions

The results of the TCAD simulations were later verified in the p-FETs with Ru-based S/D. Fig. 4.3 presents the g_m profiles of an E-mode p-FET and a D-mode p-FET (experimental results). For reference, the device structures are drawn in Fig. 4.4.

First, the g_m characteristics of the D-mode p-FET are examined. Fig. 4.3(a) shows the g_m curves at several V_{DS}. It is a well-known fact that g_m peak value increases with a more negative V_{DS} (for p-FETs; for n-FETs, a more positive V_{DS}), and the experimental results agree with this trend. The g_m peak ratio between peak 2 and peak 1 (attributed to Channel 2 and Channel 1, respectively) shows that, at a more negative V_{DS}, this ratio increases. This seems to suggest that the larger electric fields (exerted by the more negative V_{DS}) causes more effect on Channel 2 (bulk channel) relative to Channel 1 (2DHG), which could be attributed to the fact that Channel 2 is closer to the drain terminal (refer to Fig. 4.4(a) for the device structure).

Next, the g_m characteristics of the D-mode and E-mode p-FETs are compared. The characteristics as shown in Fig. 4.3(c) (experiment) closely resembles that of Fig. 4.1(b) (simulation). GR-1 and GR-3 [Fig. 4.1(b)] corresponds to E-mode, and D-mode transistors [Fig. 4.3(c)], respectively. Therefore, the TCAD simulation is experimentally validated and supports the hypothesis of the presence/absence of two component channels leading to the D/E-mode behavior and the corresponding g_m profile.

Lastly, it is noted that, the experimental results of the self-aligned short-channel p-FET are in good qualitative agreement with the simulated results of a non-self-aligned long-channel p-FET (for experimental transistor: $L_{SD} = L_G = 0.51$ µm; for simulated transistor: $L_{SD} = 6$ µm, $L_G = 2$

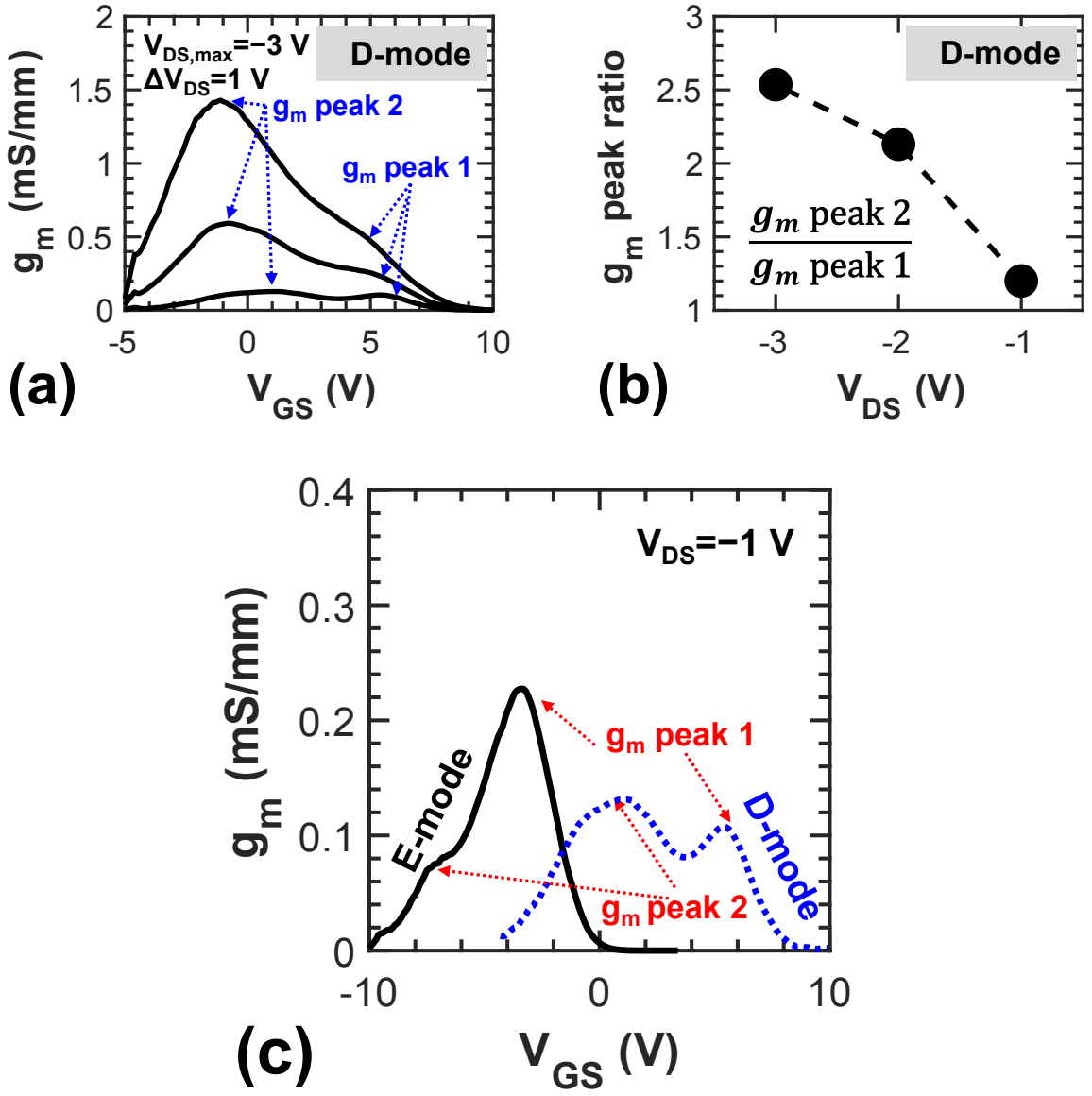


Figure 4.3: g_m of an E-mode p-FET and a D-mode p-FET (experimental results of p-FET with Ru-based S/D). (a) g_m profiles for the D-mode p-FET. (b) Ratio of g_m peaks for the D-mode p-FET. (c) Comparison of g_m profiles of the D-mode and E-mode p-FETs.

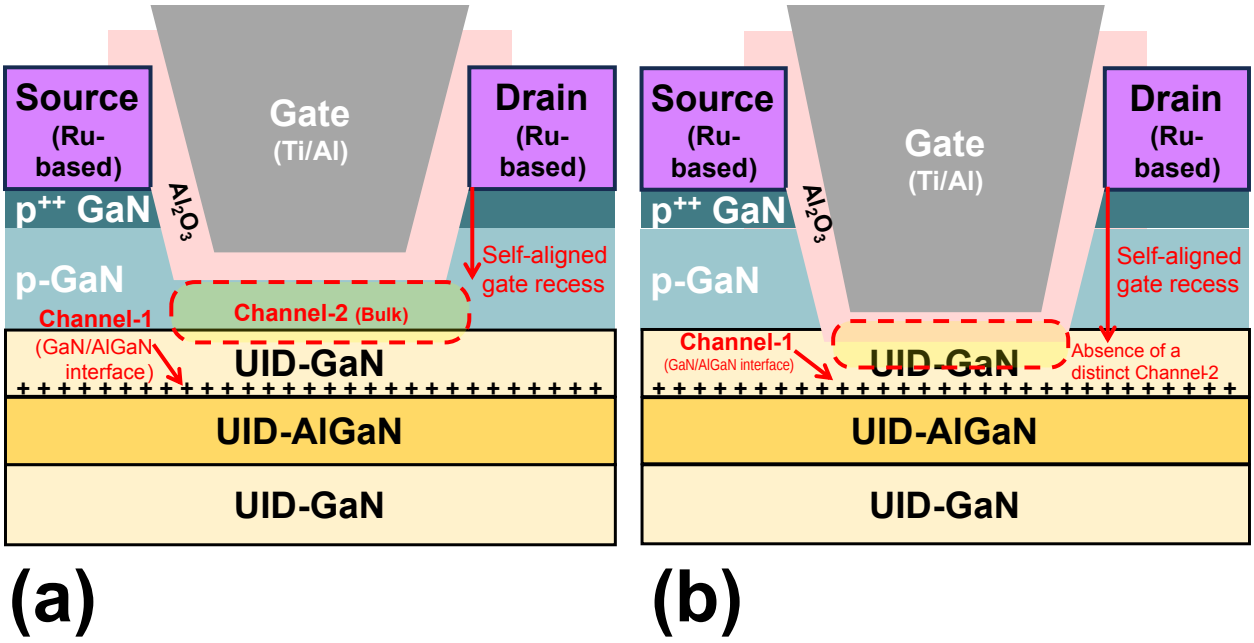


Figure 4.4: Device structures of (a) D-mode and (b) E-mode p-FETs with Ru-based S/D. The locations of Channel 1 (GaN/AlGaN interface) and Channel 2 (bulk channel) are indicated.

μm). Therefore, it suggests that the results of the TCAD simulation are broadly applicable for various p-FETs.

4.2 Impact of p-GaN Doping Profile

In most literature concerning p-FETs, for epitaxial structures involving p-doping (p-GaN/AlGaN or variants), the p-doping is usually given as a single value [57, 72, 128]. Strictly speaking, such values are the "nominal" values provided by the epitaxial grower. On one hand, these values give a convenient reference to the level of doping (e.g., 1×10^{19} cm^{-3} in the GaN-CMOS platform (bulk channel), *vs.* 3×10^{19} cm^{-3} in [57]). On the other hand, these may lead to a false impression that the p-doping profile is a uniform profile, which is certainly not the case. In the case of Mg p-doping in GaN, there are issues with the memory effect and doping delay in the growth process.

Chapter 4.1 reveals that the bulk channel plays a significant role in the operation of the p-FET. Therefore, in this chapter, the Mg doping profile in the proposed GaN-CMOS platform is characterized. Furthermore, TCAD simulations are conducted to reveal the (qualitative) impact of

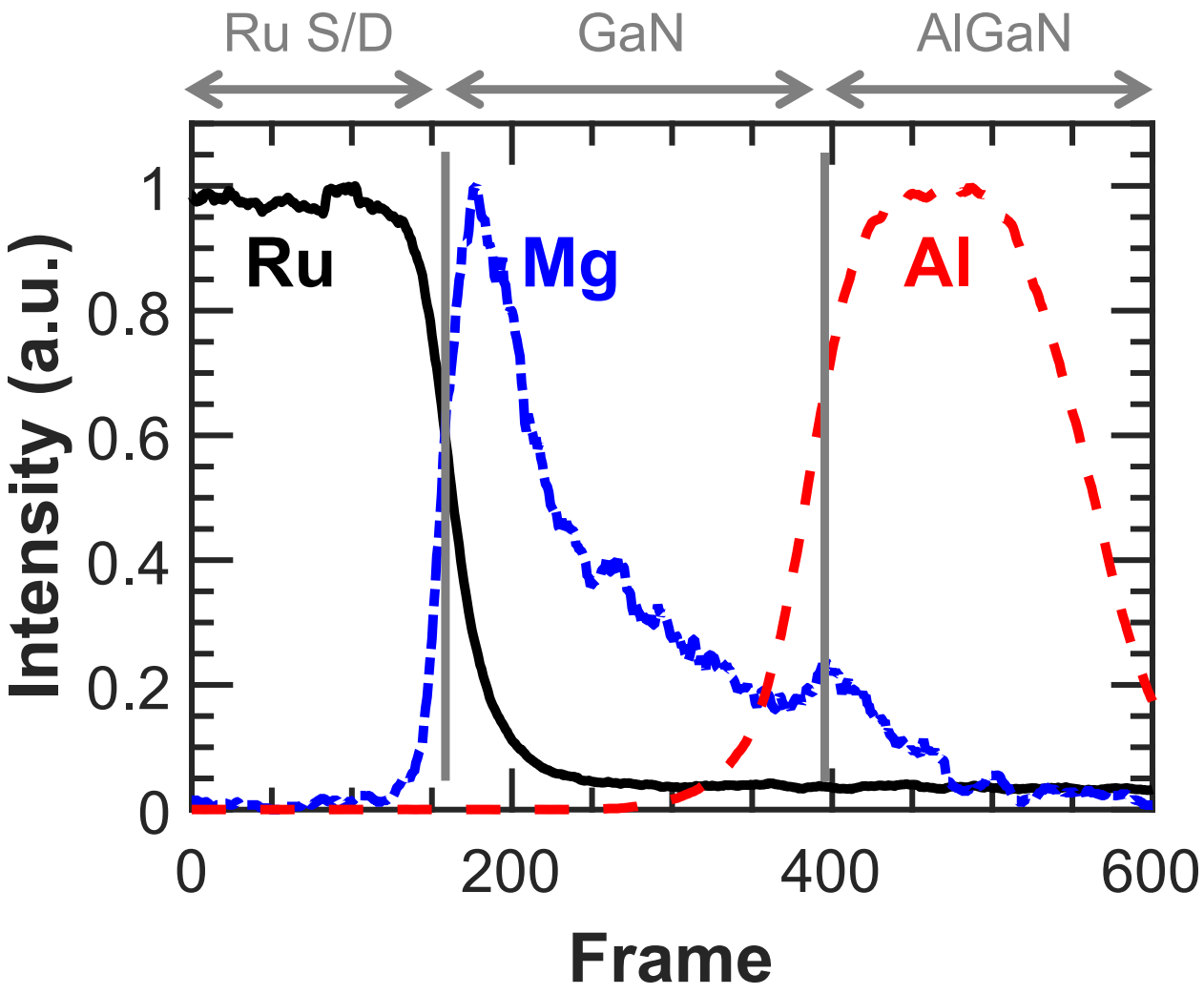


Figure 4.5: Secondary-ion mass spectrometry (SIMS) of Ru/p-GaN sample (GaN-CMOS platform). Note that each element is normalized to its own peak intensity, therefore the values of *different* elements should *not* be compared with one another. Curves are mildly smoothened to remove noisy data.

various (conceptual) Mg doping profiles on the transistor characteristics.

4.2.1 SIMS Profile of Mg Doping in p-GaN

Secondary-ion mass spectrometry (SIMS) profile of the Ru/p-GaN sample (annealed at 500 °C) was conducted. The SIMS profile is presented in Fig. 4.5. This sample corresponds to the Ru-based S/D fabricated on the GaN-CMOS platform. The interfaces between the presence of the different elements are not as sharp due to limitations with the SIMS setup and data acquisition.

The Mg profile in the III-N epitaxy roughly (and qualitatively) follows the nominal specifications provided by the supplier, which from the top, is a highly doped p^{++}-GaN layer (which is in direct contact with Ru), followed by a p-GaN layer with lower doping. It is noted that there is a linear slope even in the p-GaN layer, which could be explained by the memory effect in the Mg doping. It is interesting to note that, in this sample, the nominal UID-GaN layer still contains considerable amount of Mg (intensity is $0.15\times$ that of the p^{++} value), and in a small thickness of the AlGaN (at the top side). This indicates that there might be considerable back-diffusion (out-diffusion) of Mg in the UID-GaN and AlGaN. One would intuitively predict that, etching the entire p-GaN layer and some of the (nominal) UID-GaN layer should be sufficient to achieve E-mode, because there is no more bulk channel and a low density of 2DHG (thin UID-GaN and significant depletion by the gate). As is shall be seen in Chapter 5.1, the considerable concentration of Mg doping in the (nominal) UID-GaN layer has significant implications on the performance of such p-FETs at HT. The impact of Mg out-diffusion on p-FETs has also been studied (with a focus on V_{th} at room temperature) using 1D band diagrams [129].

4.2.2 Impact on the Performance of the p-FET (Simulation Study)

Having highlighted the issue of non-ideality in the Mg doping profile, it is imperative to study the impact on the performance of p-FETs. Furthermore, it is noted that the previously simulated epitaxial structure (Epi-1) is a custom-grown stack whose specifications deviate from the conventional structures used in (commercial) p-GaN HEMTs. In contrast, an epitaxial structure based on the existing commercially grown p-GaN/AlGaN/GaN wafers would be highly desirable in order to evaluate the potential of the proposed GaN CMOS power technology, as well as to facilitate the eventual technology transfer to commercial entities.

This difference in the doping profiles in the p-GaN would evidently affect the p-FETs more than the n-FETs. This is because the p-FETs directly rely on the p-GaN as its channel (bulk channel, as well as the role of p-GaN in forming the 2DHG), whereas for n-FETs, the p-GaN is used only to deplete the n-channel. Considering that the eventual aim of these epitaxial structures is to realize

p-FETs, it would be necessary to bring the epitaxial structure simulation to the device-level.

Therefore, the TCAD simulation framework developed in Chapter 4.1.1 would serve as a useful tool. Silvaco ATLAS was used to study the differences in doping profiles. Here, a proof-of-concept simulation was conducted using a long-channel p-FET ($L_G = L_{GS} = L_{GD} = 2$ µm) was simulated as a proof-of-concept and for ease of convergence. It is worthy to note that, through channel length scaling, current levels could be improved significantly in p-FETs. A simplified mobility model with a constant low-field hole mobility of $\mu_p = 20$ cm^2/V$\cdot$s is defined. The impact of doping on the low-field mobility (i.e., $\mu_p(N_A)$) was not included due to lack of accurate experimental data. Nevertheless, with sufficient material characterization, built-in models could be used with proper calibration of model parameters. In Silvaco, the models include the Albrecht Model (`albrct` [130]) and Farahmand Modified Caughey Thomas Model (`fmct` [131]).

In this section, a p-GaN (100 nm) / $Al_xGa_{1-x}N$ (15 nm, $x = 0.2$) / GaN epitaxial structure, which resembles a commercially grown design, is used, as shown in Fig. 4.6(a). In this epitaxial structure, the two layers which have significant flexibility in design are the p-GaN and AlGaN layers. While the impact of $Al_xGa_{1-x}N$ parameters (Al composition (x) and thickness) are well studied, primarily for p-GaN-gate HEMTs [132], the impact of the p-GaN layer requires more understanding. The device structure (similar to Chapter 4.1.1) is presented in Fig. 4.6(b).

Two doping profiles are studied in this simulation work. The first doping profile is the uniform doping profile at 1×10^{19} cm^{-3} (which is the value of the p-GaN bulk channel, in the GaN-CMOS epitaxy), which is the the assumption if the doping values (nominal) reported in the p-FET literature were to be taken at face value. The second is a linearly increasing doping profile, which takes into account the memory effect in Mg doping. This profile is the linear fit of SIMS data obtained from a representative p-GaN/AlGaN/GaN wafer. For convenient reference, the first and second profiles are named as "ideal" and "realistic" profiles, respectively. These profiles are presented in Fig. 4.7(a).

The impact of the doping profile at the material-level (band diagram and spatial charge distribution) are then studied using a 1D Schrödinger-Poisson solver (in a commercial software,

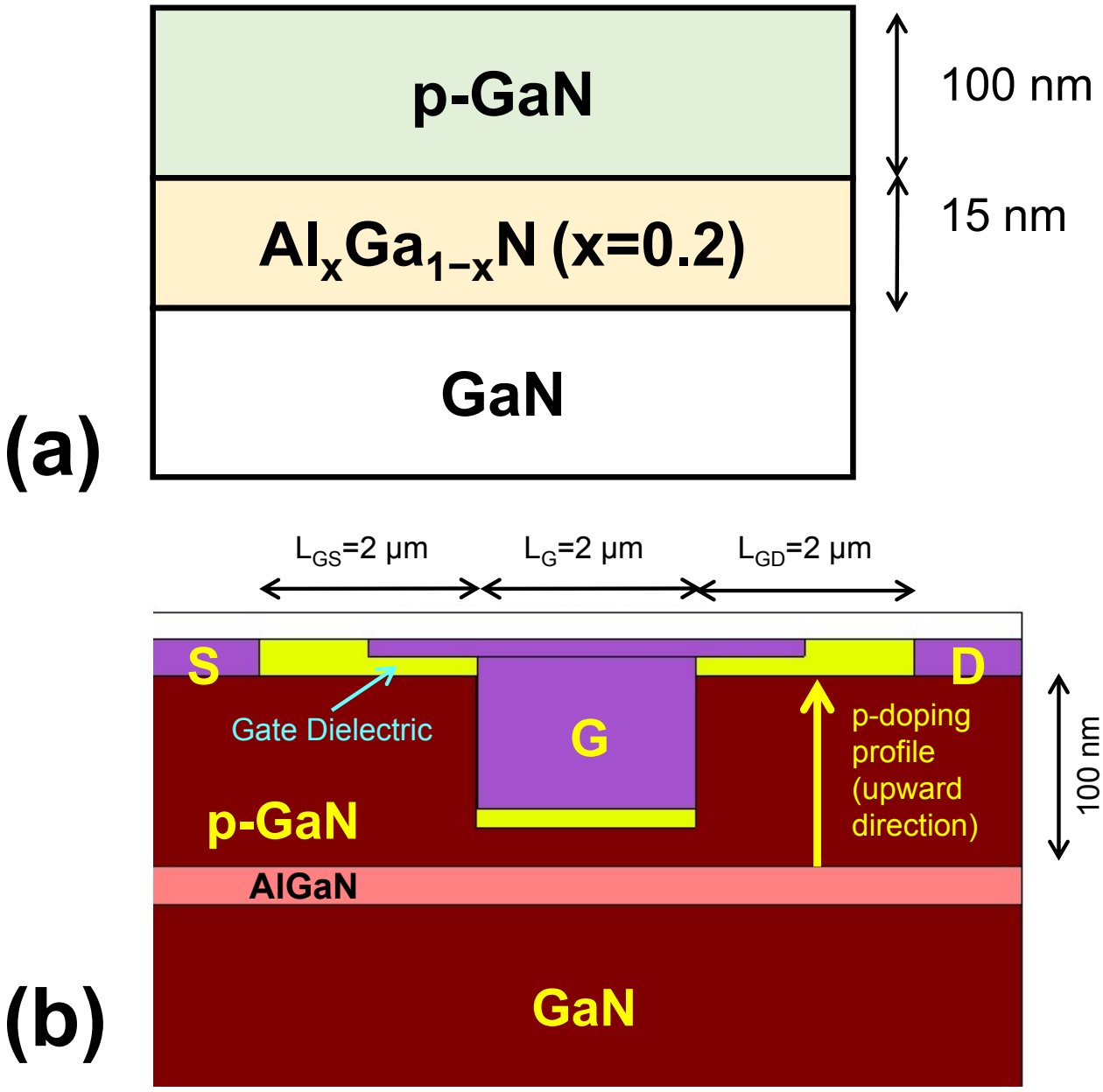


Figure 4.6: TCAD simulation setup for studying the impact of the p-GaN doping profile. (a) Epitaxial structure, consisting of a p-GaN/AlGaN/GaN epitaxial structure, similar to the conventional p-GaN epitaxy for commercial power HEMTs. (b) Device structure of the p-FET. The "upward direction," which will be referred to in Fig. 4.7, is labelled here.

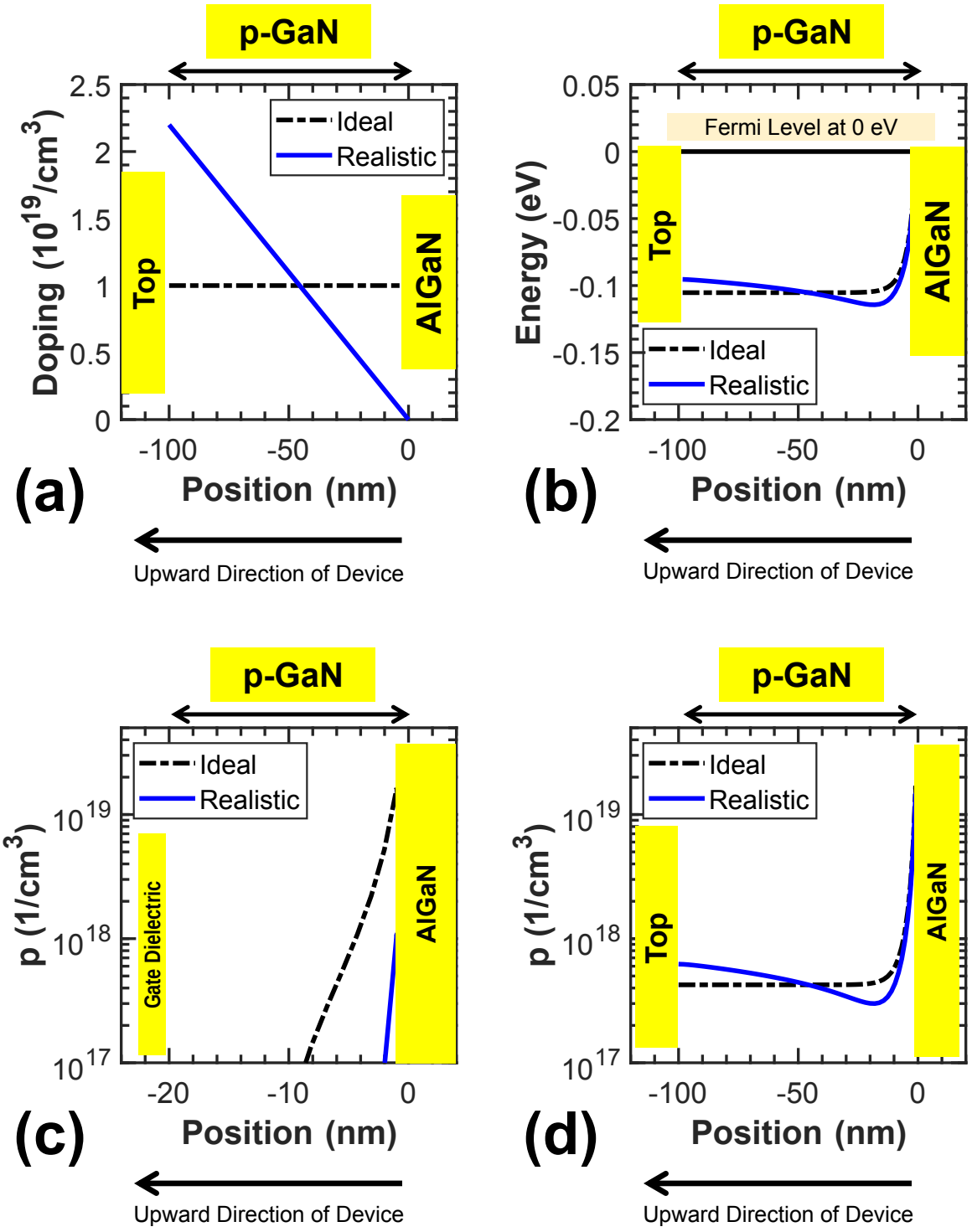


Figure 4.7: Impact of a realistic p-GaN doping profile at the material-level. (a) Comparison between the "ideal" doping profile (uniform doping of 1×10^{19} cm^{-3}) and a "realistic" doping (linearly increasing doping at a rate of 2.2×10^{17} cm^{-3}/nm of p-GaN). (b) Band diagram of the two profiles. For brevity, only the valence band is shown. (c) Hole concentration in the gated region (assuming 20 nm of GaN remaining after gate recess). (d) Hole concentration in the access region. In all the graphs, the interface of GaN/AlGaN is set as the position origin, and the upward direction of the device is indicated.

Table 4.1: Comparison of the simulated characteristics of the p-FET using a realistic p-doping profile (as compared to the ideal profile).

Observation in p-FET with realistic p-doping profile	**Explanation**
Double turn-on	Two components of the p-channel: bulk p and 2DHG
Less obvious double turn-on	Lower concentration of 2DHG
The apparent V_{th} is more negative (towards E-mode)	Less hole concentration in the gate region
Better ON-OFF ratio	(Same as above)

NextNano) and then verified when the epitaxial structure is imported in Silvaco ATLAS. Visible differences in the valence band levels could be seen in Fig. 4.7(b). The resultant hole concentrations (assuming $\Delta E_A = 0.15$ eV) for the gate region and the access region are shown in Fig. 4.7(c)–(d). The ideal profile gives a higher peak concentration at the p-GaN/AlGaN interface, which corresponds to the 2DHG. Furthermore, at ~ 20 nm from the p-GaN/AlGaN interface, the realistic p-doping profile shows a lower hole concentration, which will have implications for the p-FET characteristics.

The DC IV characteristics of the p-FETs are simulated. In terms of the output characteristics (Fig. 4.8(a)–(b)), the p-FETs with ideal and realistic profiles show similar $I_{D,max}$. Note that the simulated p-FET structure is long-channel ($L_{GS} = L_G = L_{GD} = 2$ µm), therefore a relatively low current density < 10 mA/mm was obtained. In the fabricated transistors, channel length scaling could be readily adopted to increase the current density. Nevertheless, the simulation serves as a proof-of-concept study for the impact of the doping profile. A long-channel transistor structure would be more suitable because they avoid complicating the transistor performance with short-channel effects.

As discussed in Chapter 4.1, transfer characteristics are informative for the operation of p-FETs. As shown in Fig. 4.8(c), the p-FET with a realistic p-doping profile achieves E-mode operation, while the p-FET with an ideal p-doping profile shows D-mode operation. This could be attributed to the relatively less hole concentration in the gate region (close to p-GaN/AlGaN interface) at zero bias (refer to Fig. 4.7(c)). A similar observation is obtained in ON-OFF switching,

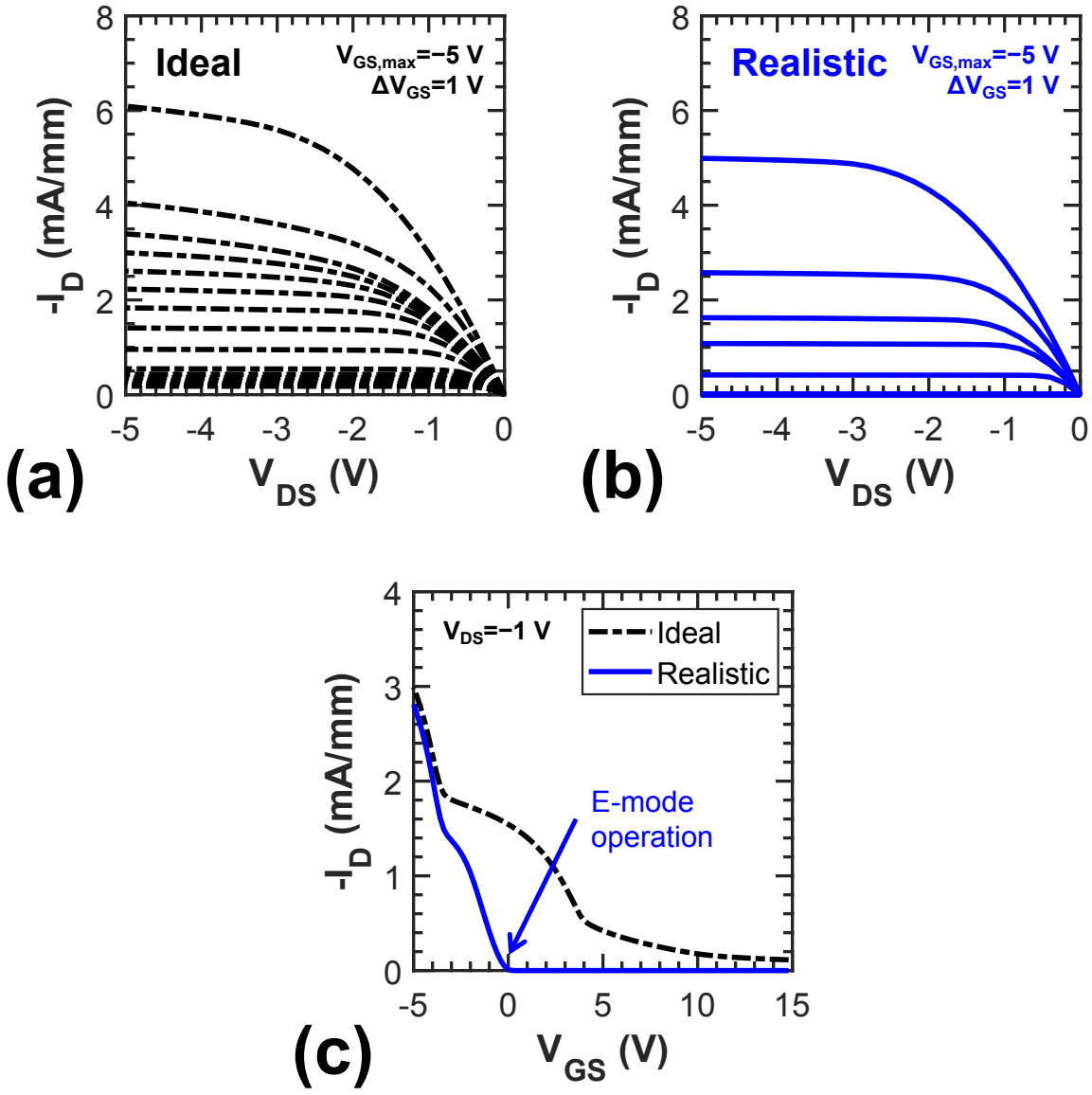


Figure 4.8: Simulated DC characteristics of the p-FET with an ideal *vs.* realistic p-GaN doping profile. (a) Output characteristics of the p-FET with an ideal p-GaN doping profile. (b) Output characteristics of the p-FET with a realistic p-GaN doping profile. (c) Comparison of the transfer characteristics between these two p-FETs.

where (from the ON-state) a larger voltage range is required to fully turn off the p-FET with ideal characteristics.

The main trade-offs and their brief explanations are presented in Table 4.1. Among the various characteristics of the p-FET with realistic p-doping, the major highlight is that, the relatively low hole concentration at the p-GaN/AlGaN interface enables the realization of E-mode and better gate electrostatic control.

In summary, the impact of p-doping profile on the p-FET performance is studied using two conceptual profiles, namely the uniform doping (ideal profile) and the linear doping (realistic profile). The study reveals that the doping profile plays a considerable role in the characteristics of the p-FET. As far as possible, the realistic p-doping profile should be used in p-FET simulations to study the mechanisms of the p-FET, in particular in the gate region.

As a concluding remark, there has been some studies on the engineering of p-doping profiles for p-GaN-gate HEMTs [133]. Such studies, while dependent on the growth conditions, would also be valuable for p-FETs. A desired p-doping profile for p-GaN/AlGaN p-FETs could be, low doping near the p-GaN/AlGaN interface (for better gate control, and higher mobility due to reduced impurity scattering), while maintaining very high doping $> 5 \times 10^{19}$ cm^{-3} at the top for the formation of ohmic contacts of p-FETs. Of course, the implications of such a p-doping profile on the n-FET (p-GaN-gate HEMT) needs to be carefully studied, as discussed in Chapter 2.4.3.

4.3 Conclusion

In this chapter, a deeper understanding of p-FET operation and characteristics was obtained through the complementary methods of experiment (measurement) and TCAD simulation. To the best of the authors' knowledge, many of the phenomena are reported and explained for the first time (e.g. "double g_m peak" as a function of gate recess, analysis of components of resistance *vs.* temperature). The results are aligned with earlier experimental observations (e.g. impact of gate recess) both by the author and other authors, while providing explanations from the aspect of transistor

mechanisms. Specifically, the "double g_m peak" behavior is attributed to the presence of two sub-channels at the GaN/AlGaN interface and in bulk GaN. The prediction from TCAD simulation studies is later verified in experiment.

Furthermore, the impact of p-doping (Mg dopant) profile in the p-GaN layer of the p-FET was studied. Considering the memory effect in Mg doping, a more realistic profile (linearly increasing doping) was adopted. The simulation indicates that there are observable differences in the p-FET performance when such a realistic profile is used (over an ideal uniform doping profile), and highlights some of the trade-offs when a realistic profile is assumed.

This study reveals unique phenomena in p-FETs, and through the analysis, allows for a better understanding of the design space of these novel transistors.

Chapter 5

p-FETs and n-FETs for High Temperature Operation

As discussed in Chapter 1.4, the characterization of p-FETs and n-FETs under high temperature (HT) is desired for reliable operation at HT (caused by a HT environment, or because of high power which leads to localized heating of the system). This chapter presents the HT performance of these transistors, with an emphasis on p-FETs based on the GaN-CMOS platform. The HT robustness of n-FETs is briefly covered, followed by the proposition of the GaN p-channel junction FET (JFET) for robust high temperature operation.

5.1 High Temperature Performance of GaN p-FETs

HT characterization of p-FETs was conducted with the following objectives: (1) to investigate the high temperature performance of these transistors and therefore evaluate its suitability for HT GaN-CMOS electronics; (2) to use HT measurements as a means to examine the hypothesis of the two sub-channels (bulk and GaN/AlGaN interface).

p-FETs based on p-GaN/UID-GaN/AlGaN/GaN and Ru S/D contacts were measured on a thermal chuck (rating of 300 °C) in a probe station. Before each measurement at each temperature set point, at least 10 min. of waiting time was implemented to ensure the device under test has reached

a uniform temperature. The temperature was raised gradually from room temperature (25 °C) to $\{100, 200, 250, 300\}$ °C.

The DC measurement results are presented in Fig. 5.1. As shown in Fig. 5.1, the transistor shows $I_{D,max}$ of -17 mA/mm ($V_{DS} = -8$ V, $V_{GS} = -10$ V). The transfer characteristics are shown in Fig. 5.1(b)–(c). Furthermore, TLMs were measured at HT in order to extract the contact resistance, which would be valuable for the analysis later.

5.1.1 Analysis of Transistor Metrics

Fig. 5.2 presents the analysis of the raw data (*vs.* temperature) shown in Fig. 5.1. $I_{D,max}$ is an important parameter for any transistor, especially for GaN p-FETs where the drive current is relatively low (compared to n-FETs), therefore coming a focus in p-FET research. Fig. 5.2(a) shows that $-I_{D,max}$ increases after 100 °C, and the value at 300 °C is 2.5 times that of the value at 25 °C. The ON/OFF ratio decreases, as shown in Fig. 5.2(b). V_{th} moves from E-mode to D-mode, as shown in Fig. 5.2(c).

In view of the above trends, several temperature-dependent factors could be considered:

1. The Mg ionization ratio significantly increases at HT because Mg is a deep level impurity. At HT, the Mg has enough thermal energy to ionize and therefore provide additional holes. This mainly affects the bulk channel (Channel 2). The assumption is that the 2DHG channel (GaN/AlGaN interface) charge density, which is induced by polarization, remains relatively constant. In the case of HEMTs, the 2DEG charge density was found to relatively constant *vs.* temperature [134].

2. The mobility of the holes decreases at HT, likely because of phonon scattering, as is also the cases for electrons.

3. The contact resistance decreases at HT, as will be examined later.

Based on the experimental results, in the case of $I_{D,max}$, the effect of higher Mg ionization ratio dominates. This directly affects the bulk channel. Consequently, the ON/OFF ratio decreases

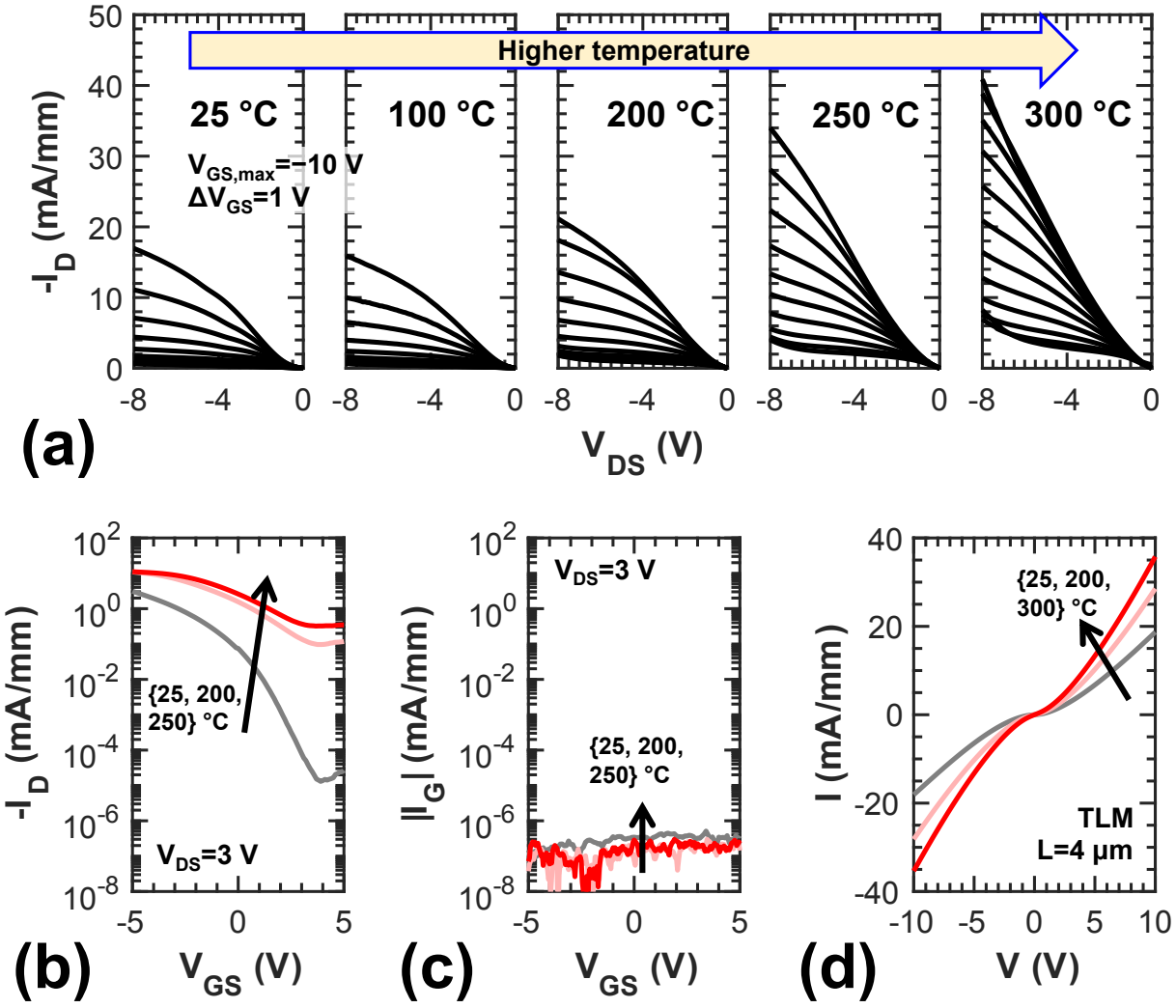


Figure 5.1: Measurement of a p-GaN/UID-GaN/UID-AlGaN/UID-GaN p-FET at high temperature up to 300 °C. (a) Output characteristics, I_D–V_{DS}. (b) Transfer characteristics, I_D–V_{GS}. (c) Transfer characteristics, I_G–V_{GS}. (d) I-V of a TLM structure.

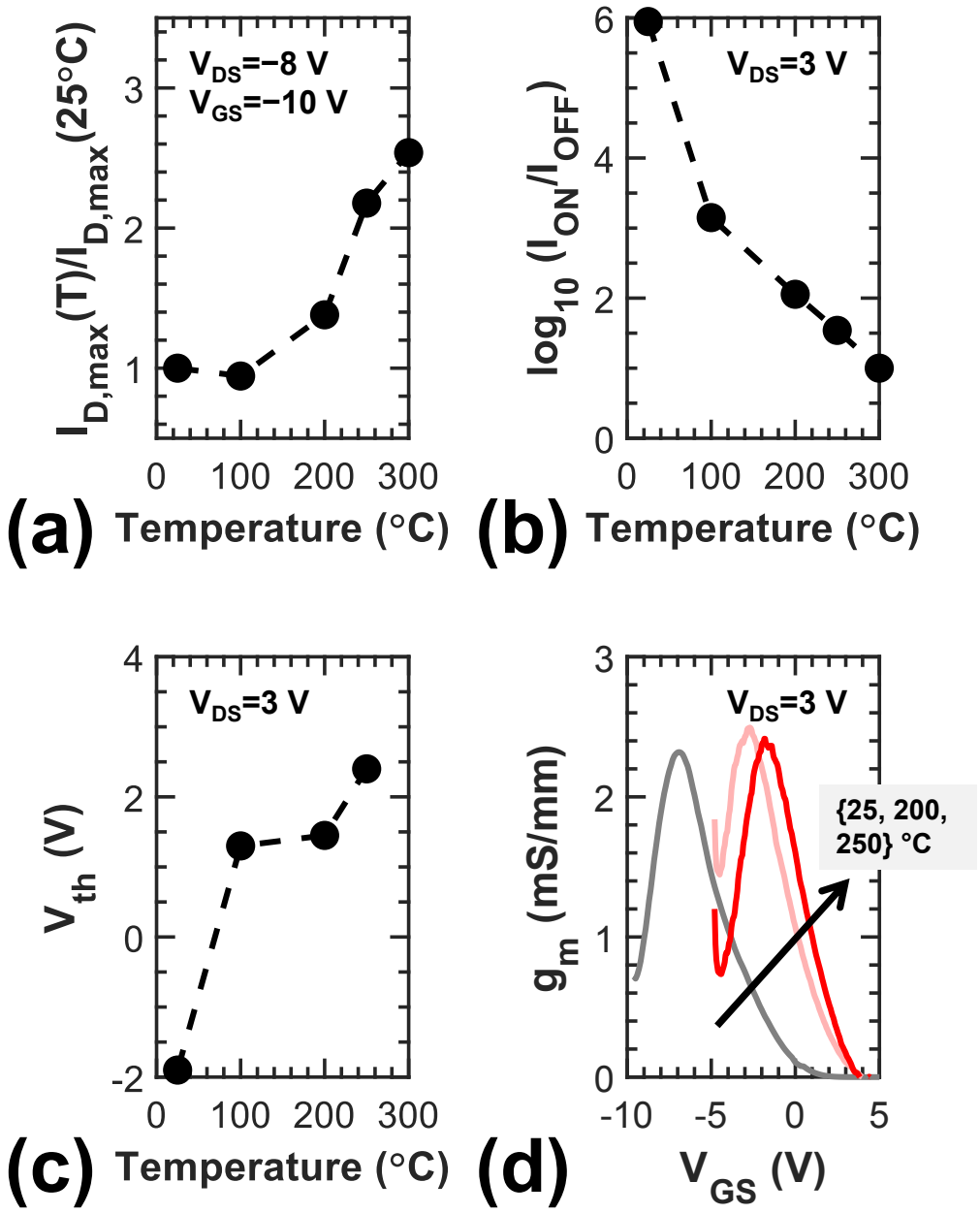


Figure 5.2: Analysis of transistor metrics and g_m at HT. (a) Maximum current density $I_{D,max}$ (normalized to value at RT, $V_{DS} = -8$ V, $V_{GS} = -10$ V). (b) ON-OFF ratio $I_{\text{ON}}/I_{\text{OFF}}$. (c) Threshold voltage V_{th}. (d) Transconductance g_m.

because it is more difficult for the gate to completely deplete the channel. The V_{th} becomes more D-mode because of the increase in charge density at zero bias. This is analagous to the situation of the (room temperature) D-mode transistor, where the main reason was the existence of a bulk p-GaN channel (remaining after gate recess).

5.1.2 g_m Characteristics

Given the earlier analysis of the unique g_m characteristics of the p-FET (Chapter 4.1), it is interesting to examine the g_m again, as shown in Fig. 5.2(d). The g_m profile at 25 °C resembles that of a typical E-mode p-FET, with only one g_m peak, corresponding to the existence of a single channel (or *de-facto* merged channel). However, with the increase in temperature, the g_m profile shows signs of a second peak. In the case of 250 °C, the first g_m peak is observed at ~ -2 V, then the g_m drops for higher gate overdrive (more negative V_{GS}), but at ~ -4.5 V, the g_m profile rises again, which will likely result in a second g_m peak for the bulk channel. Unfortunately, in the measurements at HT, the range of V_{GS} was only up to -5 V (for maximum gate overdrive). Nevertheless, the behavior resembling a double peak (as in Fig. 4.3(c)) is present in both 200 °C and 250 °C, which points to a consistent trend.

5.1.3 Re-examining the Explanations Based on Material Characterization

In the above analysis, a natural question that is related to the formation of the bulk channel arises. In Chapter 4.1, it is verified through simulation of p-FET that, in the case of a E-mode transistor (at room temperature), Channel 2 (bulk p-GaN channel) does not exist. Only the UID-GaN is remaining. However, the measurement at HT suggests that, there might be back-diffusion of Mg from the p-GaN layer into the UID-GaN layer. Such "back-diffusion" is observed also during the Mg activation annealing, which is necessary to eliminate the "Mg passivation effect" during MOCVD growth. The back-diffusion of Mg leads to a higher concentration of holes at HT, therefore resulting in the formation of a considerable bulk channel.

The (experimental) SIMS profile of the p-FET offers some answers to the discussion above.

As shown in Fig. 4.5 and as explained in Chapter 4.2.1, there is a visible concentration of Mg near the AlGaN interface, which suggests that, back-diffusion of Mg occurred in the sample. This observation is aligned with the hypothesis above.

There are several implications of the Mg doping profile at HT. The p-FET becomes more D-mode, and shows g_m characteristics which resemble the typical g_m characteristics of D-mode p-FETs (at room temperature). At HT, the Mg dopants in the nominal UID-GaN layer (which is remaining) would be activated to given higher charge density in the channel region. Consequently, the behavior of D-mode p-FETs, as presented in Chapter 4.1, emerges in these originally (at RT) E-mode p-FETs, including, increase in $I_{D,max}$, shift in V_{th} towards more D-mode, reduced ON-OFF ratio, and the iconic "double g_m peak" in D-mode p-FETs. In other words, the following two scenarios in the p-FET (from a device operation perspective) are analagous: (1) at HT, significant bulk channel due to Mg ionization (near the AlGaN interface); (2) significant bulk channel at RT due to significant remaining p-GaN/UID-GaN in the gate region.

For a more quantitative analysis, quantitative SIMS would be required (using Mg implant standards), SIMS mapping over a greater area of the p-GaN sample, and importing the SIMS profile into a TCAD process simulator. Future work could investigate how to reduce the Mg concentration near the AlGaN interface, so that the proposed p-FET could achieve normally-OFF operation at HT.

The SIMS results shown in Fig. 4.5 also confirm that, Ru has largely stayed on the sample surface, despite annealing at 500 °C (during the formation of S/D). Ru belongs to a wider class of refractory metals. This is another advantage of Ru over conventional multi-metal alloyed stacks for HT operation, because prolonged exposure to HT may cause further alloying and degradation, especially the long-term diffusion of Au [113]. Other contacts to p-GaN, e.g. Pd/Ni/Au, has been shown to experience significant degradation in the presence of a simulated Venus atmosphere (460 °C, 94 bar, CO_2/N_2/trace of SO_2) [135].

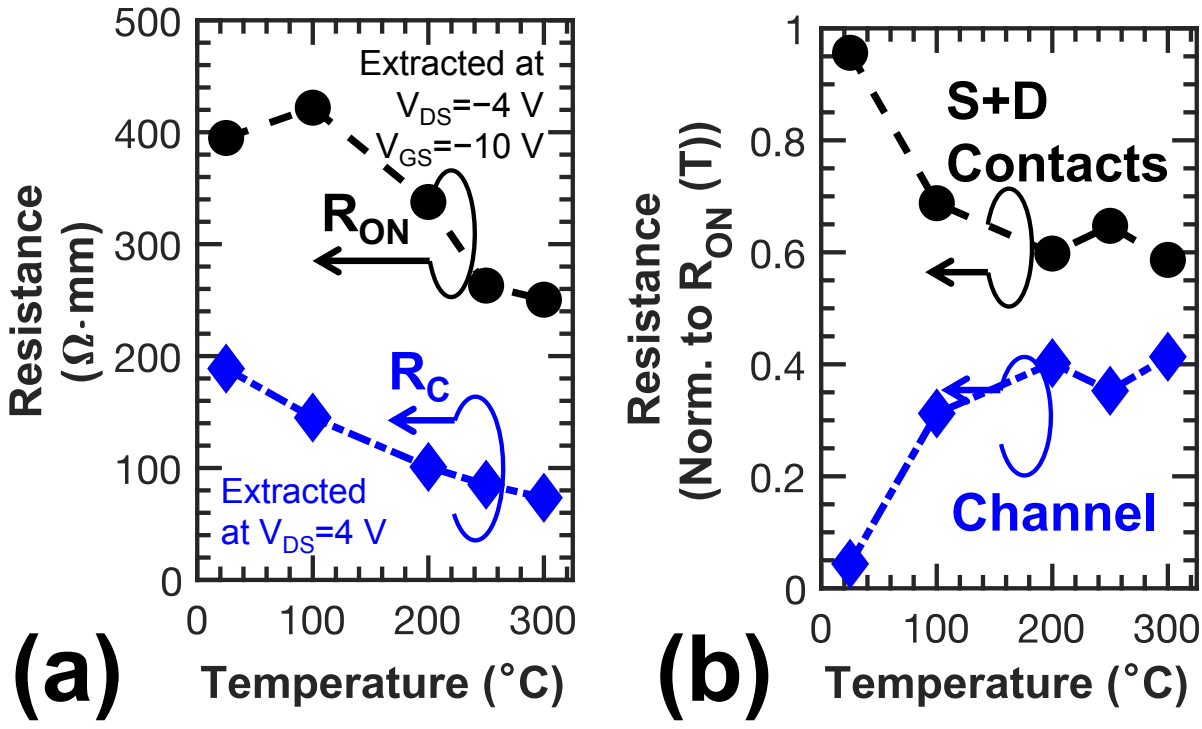


Figure 5.3: Analysis of components of R_{ON} *vs.* temperature. (a) Components of resistance (absolute values). (b) Relative proportion of components of resistance.

5.1.4 Components of ON-Resistance

It is informative to study the components of ON-resistance, given that at room temperature, the high ON of the p-FET (compared to n-FET) has been identified as a major reason (along with drive current, benchmarked in the next section, Chapter 5.1.4) for the asymmetric rise/fall time in the GaN complementary inverter [11, 26]. R_{ON} is a important metric for transistors in power applications, which is a key application area for p-FETs. Furthermore, to improve $I_{D,max}$, the components of the resistance needs to be carefully examined. Fig. 5.3(a) presents the absolute values of R_{ON} (extracted from transistor measurements (Fig. 5.1(a)), and R_c (extracted from TLM measurements). In the case of R_{ON}, a slight increase is observed at 100 °C, before decreasing at higher temperatures. This is in line with the trend of $I_{D,max}$ (Fig. 5.2(a)). The R_c decreases, because of increased thermionic emission over the Ru/p-GaN barrier.

The components of resistance are normalized to R_{ON} at the respective temperatures, as presented in Fig. 5.3(b). There are two components of resistance, namely, the source and drain contact resistance ($2 \times R_c$), and the channel resistance (R_{ch}). Due to the self-alignment between S/D and gate, negligible access region resistance is present.

At room temperature, the S/D contacts dominate R_{ON} (> 95 %). This is aligned with the author's earlier proposition of using aggressive channel length scaling as a way to minimize R_{ch}, therefore achieving overall lower R_{ON}. At this stage of research, given that the path of aggressive scaling has been repeatedly demonstrated to give low R_{ch}, the focus of p-FETs could be shifted to improving S/D contacts. Here, a variety of methods could be used, including recently reported record values using Mg-based metallization [105].

At higher temperatures, the proportion of channel resistance significantly increases. Therefore, aggressive channel length scaling is still much desired for HT operation. However, other design trade-offs need to be carefully considered. For example, short-channel p-FETs typically struggle to achieve good gate control (e.g. high ON-OFF ratio, also typical for D-mode p-FETs).

Up to this point, the DC characteristics of the p-FET have been analyzed. Looking only at

transistor-level metrics (i.e., from the circuit-level), several characteristics resemble that of the n-FET (HEMT). For example, the ON-OFF decreases at HT, in the HEMT it is because of increased gate leakage (through the Schottky barrier) at HT. The trend that is probably the most unique is the $I_{D,max}$ at HT. This is in contrast to most transistors (including GaN HEMTs), where a degradation of $I_{D,max}$ is observed [81]. On one hand, the higher drive current makes the p-FET more suitable for HT operation; on the other hand, it potentially leads to issues such as thermal runaway, which is undesired in power circuits. Therefore, if such p-FETs were to be used in power ICs, there could be additional current limiters (similar to those used to prevent electrostatic discharge).

5.1.5 Benchmarking of p-FET Performance at High Temperature

Similar to R_{ON} (discussed in Chapter 5.1.4), the drive current of the p-FET has been identified as a major cause of the asymmetric transient performance in the complementary inverter. While the I_D trend has been analyzed in Chapter 5.1.1, it is also informative to benchmark the temperature dependencies of the drive current against other reported p-FETs in the literature. There are not too many reports of the performance of p-FETs at high temperature [53, 64, 89, 103, 123, 136–139], and there are very few analyses on their trends [136]. Among the reports, the transistors with drive current $>$ 1 mA/mm at room temperature have been benchmarked in Fig. 5.4. All of these p-FETs which are shown in Fig. 5.4 are based on a p-(Al)GaN/AlGaN heterostructure, with an optional UID-GaN layer between p-(Al)GaN and AlGaN. (It turns out the reported transistors with HT data and with drive current $>$ 1 mA/mm (room temperature) are all based on such epitaxial structures.) In each benchmarking plot of Fig. 5.4, the desired corner has been identified as the region of operation at high temperature and high current.

Fig. 5.4(a) shows I_D (absolute value) as a function of temperature. To the best of the author's knowledge, the proposed p-FET of this work features the highest $-I_D$ *vs.* temperature at all temperatures, among the p-FETs whose high temperature characteristics has been reported. In fact, for the proposed p-FET, $I_D = -17$ mA/mm is a high current density for E-mode planar p-FETs (refer to Fig. 3.9(b)) considering the strong E-mode of $V_{th} = -2$ V.

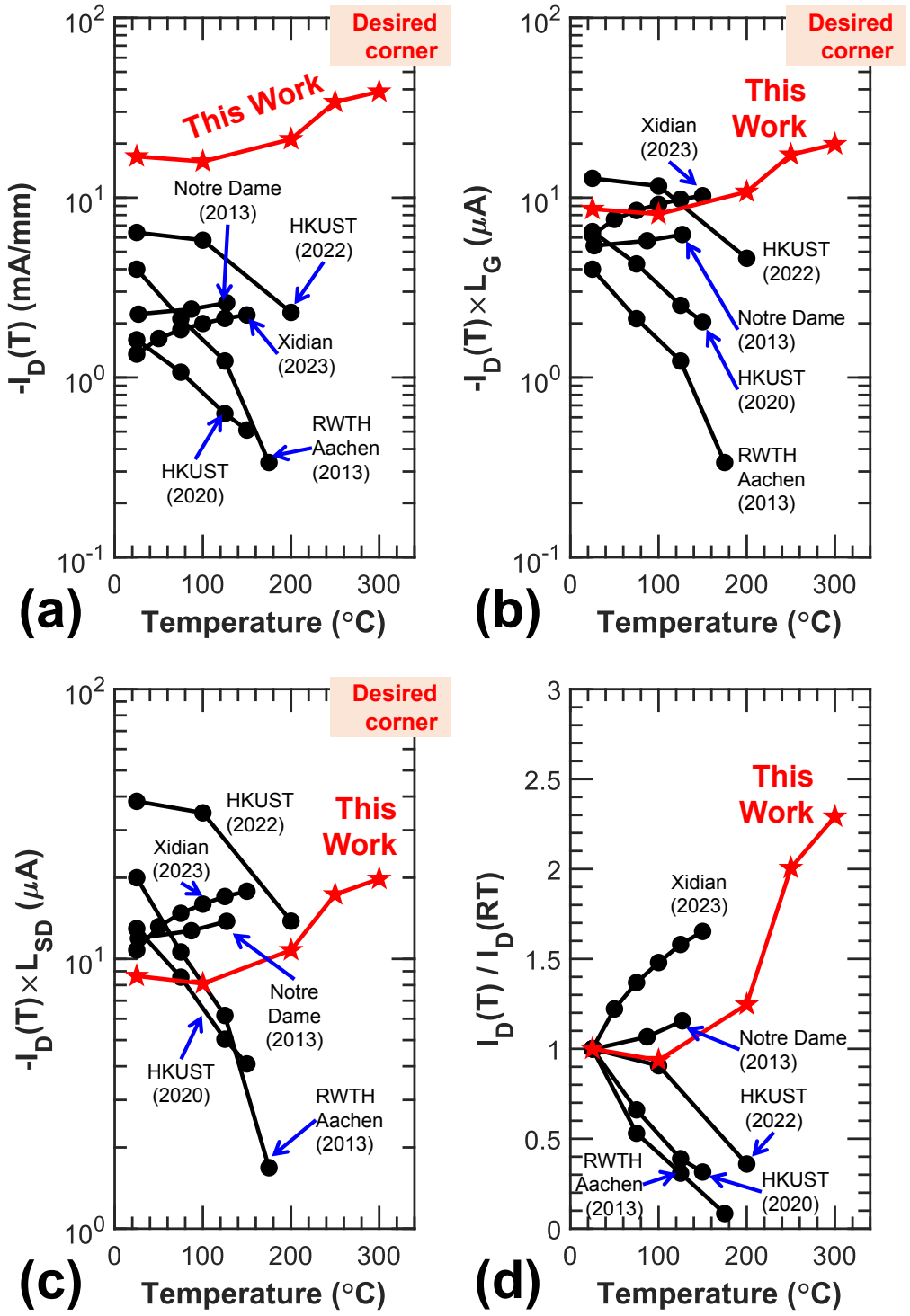


Figure 5.4: Benchmarking of p-FET performance at high temperature. (a) $-I_D(T)$. (b) $-I_D(T)$ normalized by L_G. (c) $-I_D(T)$ normalized by L_{SD}. (d) $I_D(T)$ normalized by I_D at room temperature (RT). The values of other published p-FETs are extracted from [89, 123, 136, 137, 139]. All of these p-FETs are based on a p-(Al)GaN/AlGaN heterostructure, with an optional UID-GaN layer between p-(Al)GaN and AlGaN.

Furthermore, as explained in Chapters 2.5 and 3.3, I_D of p-FET is a strong function of L_G. Earlier p-FETs have reported a $I_D \propto 1/L_G$ relationship [65]. Therefore, $I_D(T)$ of the p-FETs are normalized by L_G, as shown in Fig. 5.4(b). Similarly, as shown in Fig. 5.4(c), $I_D(T) \times L_{SD}$ is also benchmarked, because the access region also plays a role in the total ON-resistance, and some of the benchmarked p-FETs feature long L_{GD} (hence long L_{SD} for breakdown voltage considerations. In these cases, the $I_D(T)$ normalized by length metrics show that this work achieves values of $-I_D(T) \times L_G$ and $-I_D(T) \times L_{SD}$ (at HT) which are close to the desired corner.

Lastly, from a device physics perspective, it is informative to compare the relative change in I_D *vs.* temperature. Such benchmarking was previously conducted for GaN n-FETs (HEMTs) [81] to indicate relative current degradation for various n-FETs at HT. In Fig. 5.4(d), the values of $I_D(T)$ are normalized by their values at room temperature. This work exhibits an increasing trend in $I_D(T)/I_D(\mathrm{RT})$. The results could be attributed to: (1) the bulk channel in the pseudo-access regions (from ohmic contact to interface of GaN/AlGaN); (2) the remaining "UID-GaN" (nominal) layer which contains considerable Mg doping, therefore forming a pseudo-"bulk" channel with considerable charge density at HT. A comparison with another transistor with significant $I_D(T)/I_D(\mathrm{RT})$ increase at HT, labelled as "Xidian (2023)" [123] also offers some indication. In this transistor, the epitaxial structure (from top) is p-GaN (3 nm) / p-$Al_{0.05}Ga_{0.95}N$ (70 nm) / undoped-GaN (5 nm) / $Al_{0.15}Ga_{0.85}N$ (15 nm). (Nominal level of Mg doping is 3×10^{19} cm^{-3} for all p-type layers.) After the gate recess, the epitaxial structure underneath the gate stack became p-$Al_{0.05}Ga_{0.95}N$ (8 nm) / $Al_{0.15}Ga_{0.85}N$ (15 nm), which implies that a significant doped channel remained underneath the gate. This comparison suggests that the residual bulk channel is a reason for the increase in current at HT.

5.1.6 Summary on High Temperature Performance of p-FETs

In Chapter 5.1, the high temperature characteristics of a recent p-FET (with good performance at room temperature) was analyzed. The DC trends and components of ON-resistance reveal unique trends of such p-FETs at HT. A benchmarking on I_D revealed that excellent HT performance was

achieved, though there are several areas for improvement, especially in terms of ensuring good ON-OFF at HT. This work conducts a comprehensive study of the HT characteristics of a recent p-FET (with good performance). Future work could expand to include device design parameters, such as impact of gate recess, impact of access region *vs.* self-aligned architecture, impact of post-gate-recess interface to deepen the knowledge on the high temperature operation of p-FETs. Furthermore, issues such as hole transport at HT could be considered for a more quantitative analysis [140].

5.2 HT robustness of n-FETs

While this chapter mainly focuses on the p-FET, which is relatively less studied in terms of HT characteristics, work was also conducted on the HT robustness of the n-FET (p-GaN-gate HEMT). These p-GaN-gate HEMTs were fabricated on the conventional p-GaN epitaxy (Epi-2). These include [94, 141]:

1. Temperature-dependent studies of the drive current up to 500 °C, through probe station measurements of the transistor, TLM analysis, and Hall measurements;

2. *In-situ* measurement of the transistor in a simulated Venus environment (460 °C, 94 bar, $CO_2/N_2/SO_2$). Data analysis of the electrical measurement data was conducted, which revealed the "burn-in" effect.

3. Analysis of the advanced microscopy of the p-GaN-gate region, which enables E-mode operation of the n-FET, after the harsh environment test. A p-GaN/AlGaN/GaN heterostructure was maintained, as reflected in the smooth interface between the epitaxial layers, and the crystallinity in p-GaN.

4. Material characterization of the device after the harsh environment test, which revealed the effectiveness of the SiO_2 protective layer.

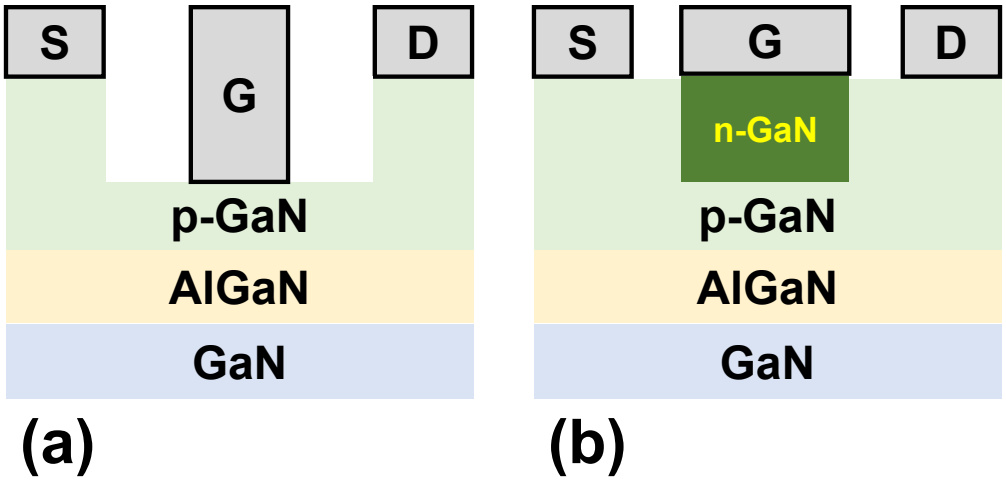


Figure 5.5: Concept of the (a) Schottky gate (MESFET) and the (b) p-n junction gate (junction FET) for p-FETs. These are two gate structures which do not require gate dielectric.

5. Experimental measurements of stress in the films and simulations reveal that the source of structural degradation in the p-GaN-gate region is the coefficient of thermal expansion (CTE) mismatch, mainly between the tungsten gate and the SiO_2 layer.

5.3 Exploration of Alternative Transistor Structures for High Temperature Robust p-FETs

While the p-FET reported in Chapter 5.1 has shown good performance among its counterparts published in the literature, a major concern is the presence of gate dielectric. On one hand, the gate dielectric allows for a very low gate leakage, even up to 300 °C for relatively short periods of time ($<$ 1 h) (Fig. 5.1(c)). On the other hand, many n-FETs which have been demonstrated to work in harsh environments do not have gate dielectric, because their reliability and potential material degradation at HT becomes a concern [15, 142]. The insights from HT robust n-FETs shed light on the development of their HT-robust complementary counterparts, the p-FETs.

Two gate structures which avoid the use of the gate dielectric are shown in Fig. 5.5. The Schottky gate on p-GaN would form a MESFET-like structure (5.5(a)), and there has been several transistor demonstrations [57,65]. However, a common problem is the relatively high gate leakage,

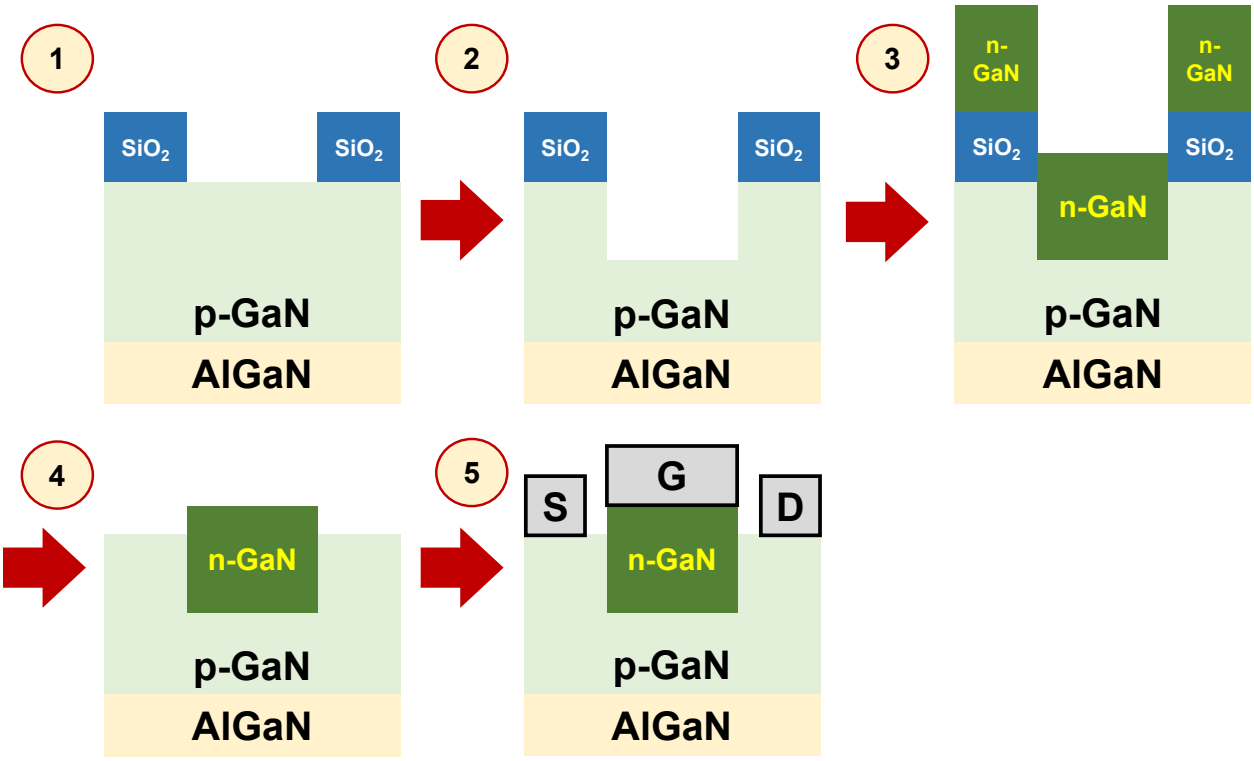


Figure 5.6: Process flow for the proposed GaN p-channel JFET, as follows: (1) Patterning of SiO_2 mask; (2) Etching p-GaN; (3) Regrowth of n-GaN; (4) Removal of SiO_2 and amorphous GaN (on SiO_2); (5) Formation of S/D metal contacts and gate metal contact.

because it is difficult to find an extremely good Schottky metal to p-GaN (a very low workfunction metal would be required). Another option, as illustrated in Fig. 5.5(b), where the p-n junction forms a potential barrier in the gate region to form a Junction FET (JFET). JFETs are widely used in SiC HT technology [143–145].

Fig. 5.6 illustrates a proposed process flow for the GaN p-channel JFET concept. The process is similar that of n-GaN regrowth for regrown ohmic contacts to 2DEG [146, 147]. SiO_2 (350 nm) is used as the regrowth mask. SiO_2 is patterned using CHF_3/CF_4 (30/30 sccm) plasma. The parameters of the recipe were a pressure of 0.5 Pa, an ICP power of 100 W, and an ICP bias of 50 W yielding an etch rate of 50 nm/min. A bi-layer ZEP520A resist (950 nm) is used as the etch mask for SiO_2 and subsequently, GaN. The p-GaN is recessed to a suitable depth (similar to gate recess), using Cl_2/BCl_3 (15/5 sccm), at an etch rate of 75 nm/min. Then, the structure is loaded into the MBE chamber regrowth of n-GaN. Prior to the actual regrowth of n-GaN, Ga is flown onto

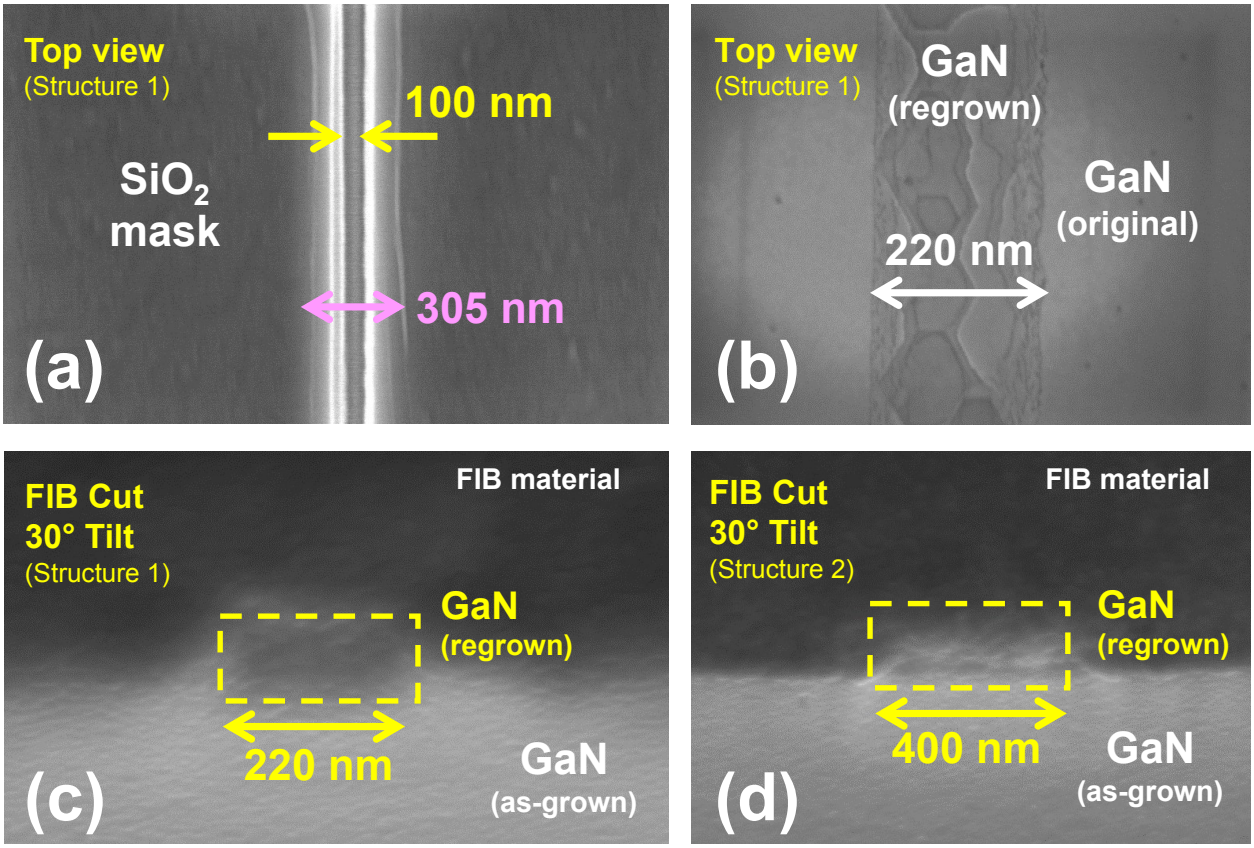


Figure 5.7: Process development for the short-channel regrowth. (a) Top view of Structure 1 after Step 2. (b) Top view of Structure 1 after Step 4. (c) Cross-sectional FIB cut of Structure 1, showing the regrown GaN region with a length of 220 nm. (d) Cross-sectional FIB cut of Structure 2, showing the regrown GaN region with a length of 400 nm. The surface of the cross-section was coated with thin (10 nm) metal to improve the contrast in the SEM imaging. The step numbers correspond to the process flow illustrated in Fig. 5.6.

the sample to desorb and remove the native oxide. n^{++} GaN (70 nm) is regrown on the sample with a Si doping concentration of $> 1 \times 10^{20}$ cm^{-3} via MBE at a growth temperature of 750 °C (T_{sub}). After the MBE step, the SiO_2 and amorphous GaN (on SiO_2) are removed by buffered oxide etch (BOE, 7 : 1) and hot (80 °C) KOH. Lastly, the S/D metal contacts are formed, followed by the gate metal contact (which is located on the n-GaN region).

In the case of the Schottky gate and junction gate, there will be higher gate leakage than in the case of the MIS gate (assuming a high quality gate dielectric) because the Schottky metal/p-GaN potential barrier and the p-n junction potential barrier are lower than the potential barrier imposed by the gate dielectric. Therefore, short-channel transistors are required in order to minimize the

gate leakage, as is shown for Schottky gate p-FETs [65]. In this work, preliminary process development was conducted on short-channel junction gates. Though AlGaN/GaN HEMT test samples were used in the process development, the developed process could be easily transferred to the actual p-GaN epitaxy. Fig. 5.7(a) shows the top view of a gate structure (Structure 1) after Step 2. After the regrowth and lift-off, in Step 4, the regrown GaN is shown in Fig. 5.7(b)–(c), where $L_G = 220$ nm is obtained. A similar structure (Structure 2) with a longer $L_G = 400$ nm is shown in Fig. 5.7(d).

The results of the process development indicate that the proposed p-channel JFET is entirely feasible from a fabrication point of view. Future work could include optimization of gate recess and detailed study of the interface between the as-grown p-GaN and the regrown n-GaN.

5.4 Conclusion

The high temperature characterization of the p-FET revealed the relative role of the two channels *vs.* temperature, and the trends in transistor performance at HT. This study enhances the appreciation of the design space of the p-FET for high performance in room temperature and HT operation. The n-FET was also examined for its robustness and sources of degradation after harsh environment exposure. Preliminary process development for the proposed p-channel JFET was conducted. The results, taken together, make the proposed GaN complementary technology a promising candidate for HT electronics.

Chapter 6

Towards DTCO in high temperature GaN-on-Si technology: a CAD framework up to 500 °C

The materials in this chapter are partially based on the following publication. The published materials in the publication mentioned below are reused with permission.

Q. Xie *et al.*, "Towards DTCO in high temperature GaN-on-Si technology: Arithmetic logic unit at 300 C and CAD framework up to 500 C," *2023 Symposium on VLSI Technology and Circuits*, Jun. 2023. © 2023 The Japan Society of Applied Physics [148]

6.1 Introduction

Experimental research of GaN high temperature (HT) electronics have thus far has focused on proof-of-concept HT GaN transistors and circuits, based on a variety of logic families (Enhancement / Depletion-mode n-FET, complementary n-/p-FETs etc. [26, 53, 80]), transistor technologies (p-GaN-gate, fluorine-plasma etc. [23, 80]), and integration (monolithic or heterogeneous [149]).

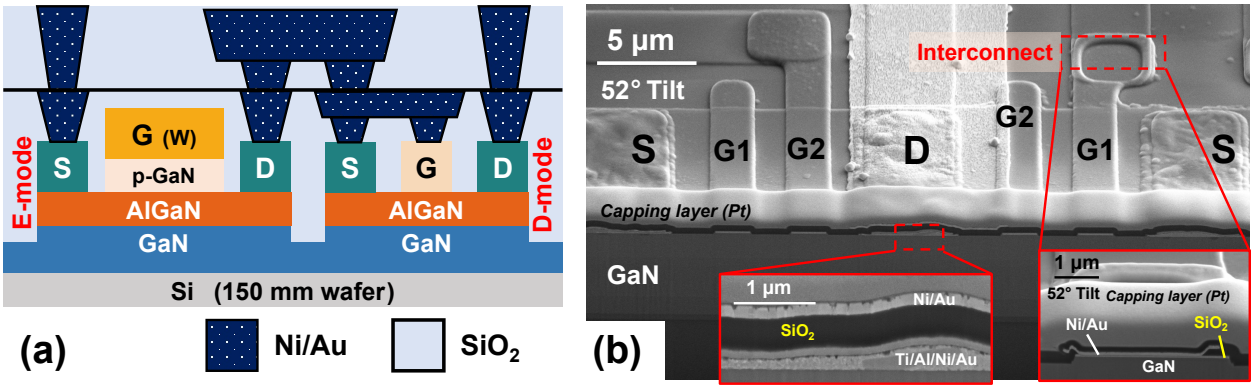


Figure 6.1: (a) Proposed GaN high temperature (HT) technology based on an E/D-mode GaN-on-Si platform. (b) Tilted view shows the device structure and the cross-section (focused ion beam cut) of the fabricated circuit. Double-gate transistors are presented. The metal stack and interconnect are presented in the insets.

However, more research effort is required on: (1) improving the performance of HT circuits; (2) accessing the long-term robustness of the transistors; (3) monolithic integration on a scalable platform to accelerate commercialization; and (4) leveraging computer-aided design (CAD) framework to achieve rapid scaling-up and reduce time-to-market.

6.2 Technology Foundation

The HT GaN technology used in this work (Fig. 6.1) stands out thanks to (1) state-of-the-art propagation delay $t_p \propto L_G^2$ at 25 °C and operational at 500 °C (highest temperature of GaN ring oscillators (ROs)) [80]; (2) long-term robustness in harsh environment [81, 94]; (3) monolithically integrated on 150 mm GaN-on-Si platform [74]. The technology is based on E/D-mode n-FETs, where the E-mode driver is the p-GaN-gate AlGaN/GaN high electron mobility transistor (HEMT) and the D-mode load (gate-source tied) is the AlGaN/GaN HEMT. A refractory metal (tungsten) self-aligned gate process is used to achieve high uniformity and eventual scaling for HT, high-speed applications [71].

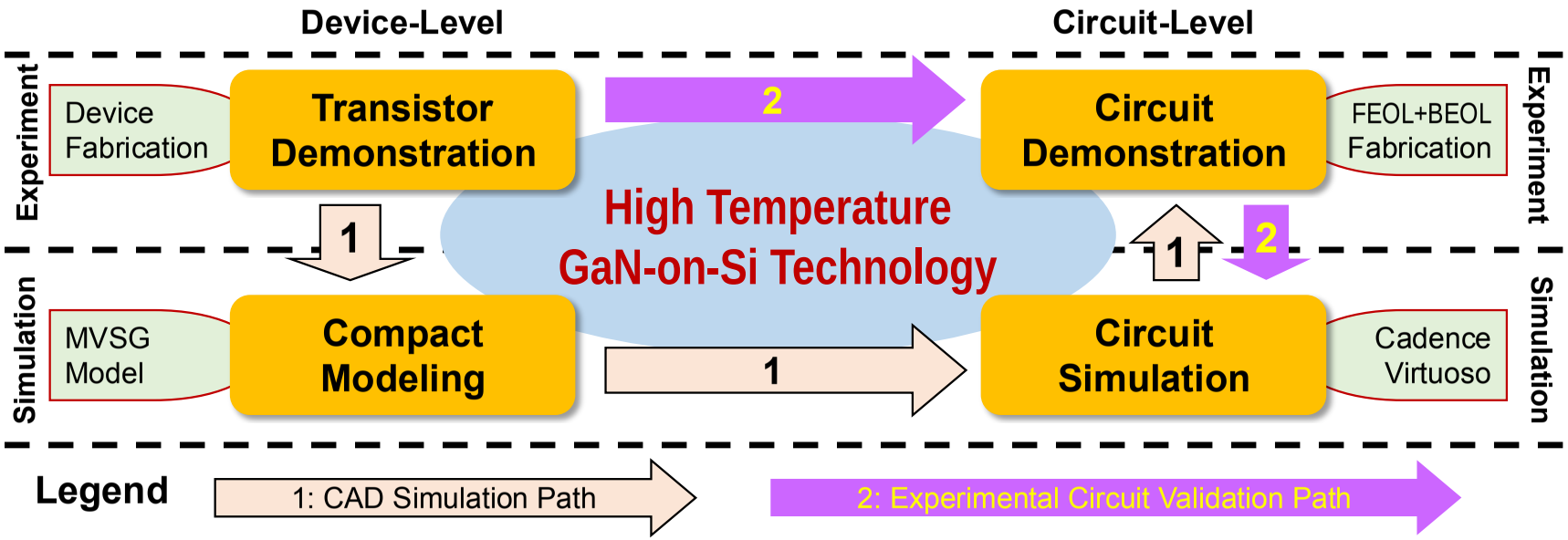


Figure 6.2: Methodology for the research of the proposed GaN HT technology. The green shapes indicate the key task or tool necessary for the accomplishment of each module. The numbered arrows indicate the two complementary pathways adopted in this work to scale up the proposed technology.

6.3 Methodology

Using complementary approaches of experiment and simulation, this work advances a roadmap for the proposed technology (Fig. 6.2). Earlier studies are mainly concerned with the performance projection of novel GaN transistors, therefore a three-step methodology was adopted [39,69,150,151], namely, (1) transistor TCAD simulation / experimental measurement, (2) compact modeling, (3) simulation of basic circuits (e.g., logic inverter, Class AB power amplifier). In this work, an "experimental validation path" was added, where the circuits were fabricated and compared with the simulation results. This would allow for experimental validation/calibration of the simulation framework (as opposed to merely "performance projection"). In this work, four sections are covered, namely:

1. Transistor demonstration (device-level, experiment)
2. Compact modeling (device-level, simulation)
3. Circuit simulation (circuit-level, simulation)
4. Circuit demonstration (circuit-level, experiment)

At the core of the simulation framework is a novel computer-aided design (CAD) framework that is then calibrated with experimental data at both the device-level (HT transistors) and circuit-level (more complex circuits, e.g. arithmetic logic unit (ALU)). The differences between the simulation and experimental circuits are used to provide feedback on future improvements to the proposed technology.

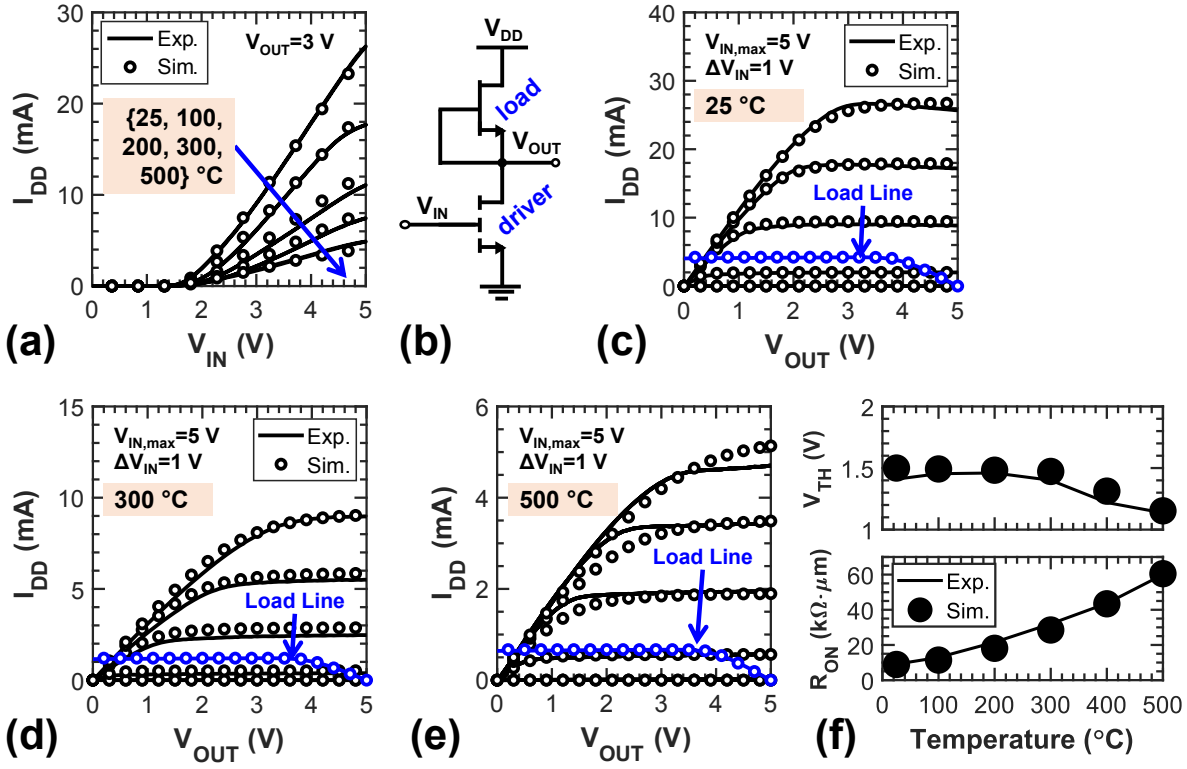


Figure 6.3: Characterization and compact modeling of the transistors up to 500 °C. Industry-standard MIT Virtual Source GaN Transistor Model (MVSG) was used. (a) Transfer characteristics of the E-mode transistor (driver, $W/L = 36/2$ μm/μm). (b) E/D-mode inverter. (c)–(e) Output characteristics of the driver with the load line (D-mode transistor, $W/L = 12/2$ μm/μm), at $\{25, 300, 500\}$ °C, respectively. (f) Summary of the key parameters of the driver transistor, V_{TH} (calculated by linear extrapolation at $V_{DS} = 3$ V) and R_{ON} (calculated at $V_{GS} = 5$ V, $V_{DS} = 0.1$ V). Excellent fit was achieved using a single model for each type of transistor across a wide temperature range.

Table 6.1: MVSG model parameters.

Parameter \ Transistor Type (n-FET)	E-Mode	D-Mode
C_g $\left(\mathrm{nF/cm^2}\right)$	2.75	3.50
$v\left(T_0\right)$ $\left(10^6\mathrm{cm/s}\right)$	6.5	10
v_ζ $\left(10^3/\mathrm{K}\right)$	1	1
$\mu\left(T_0\right)$ $\left(\mathrm{cm^2/V\cdot s}\right)$	220	550
$R_{sh}\left(T_0\right)$ $\left(\Omega/\square\right)$	1050	920
$R_c\left(T_0\right)$ $\left(\mathrm{k\Omega\cdot\mu m}\right)$	1.1	1.1
R_1 $\left(10^{-3}/\mathrm{K}\right)$	1	6
R_2 $\left(10^{-6}/\mathrm{K^2}\right)$	22	3.6
$SS\left(T_0\right)$ $\left(\mathrm{mV/dec}\right)$	110	110
$V_{TH}\left(T_0\right)$ $\left(\mathrm{V}\right)$	1.5	-1.6
$V_{TH\zeta}$ $\left(10^{-4}\ \mathrm{V/K}\right)$	1	-2
$V_{TH\zeta 2}$ $\left(10^{-3}\ \mathrm{V/K}\right)$	-1.6	0

6.4 Experimentally Verified CAD Framework for HT GaN-on-Si Technology

A CAD framework of the proposed technology would serve as a first step towards the scaling up and eventual design technology co-optimization (DTCO). A unique challenge in this framework is the need for modeling and validation over a wide temperature range, given that this framework is intended for high temperature application. To this end, a HT-enhanced version of the industry-standard MIT Virtual Source GaN Transistor Model (MVSG) [152] was adopted to achieve excellent fit up to 500 °C (Fig. 6.3).

Table 6.1 presents 6 key MVSG parameters with up to second-order temperature dependencies. The temperature dependencies are reflected in (based on the formulation of the MVSG): (1) electron source injection velocity, (2) low-field mobility, (3) sheet resistance, (4) contact resistance, (5) sub-threshold swing (SS), (6) threshold voltage. Some variables are considered to be constant *vs.* temperature, for example, gate capacitance C_g. Hall measurements suggest that the 2DEG sheet charge density has remained largely constant from room temperature to $>$ 500 °C [134]. The ge-

ometry in the gate region is independent of temperature, therefore, it may be assumed that, to the first order, C_g remains relatively constant. In fact, the fact that the MVSG is largely physics-based is an important consideration in the choice of compact model for high temperature applications.

The E-mode transistor features a unique trend in V_{TH} due to its p-GaN-gate. A slightly increasing V_{TH} was found up to 300 °C. This could be attributed to the increasing ionization ratio of Mg (acceptor) in p-GaN, therefore leading to further depletion of the 2DEG in thermal equilibrium. However, above 300 °C, the V_{TH} was found to decrease, because of a lower turn-on voltage of the p-i-n junction (in p-GaN-gate) and a reduced Schottky barrier (gate metal/p-GaN) height [153]. Therefore, to accommodate this unique behavior of the E-mode p-GaN-gate HEMT, a two-part equation (6.3) for V_{TH} was inserted in the enhanced MVSG, as shown in Eq. (6.1).

$$V_{TH}(T) = V_{TH}(T_0) + V_{TH\zeta} \times (T - T_0) + V_{TH\zeta 2}(T) \times (T - T_1) \tag{6.1}$$

$$V_{TH\zeta 2}(T) = \begin{cases} 0 & \text{if } T \leq T_1 \\ V_{TH\zeta 2} & \text{if } T > T_1 \end{cases}$$

where $\{T_0, T_1\} = \{25, 300\}$ °C.

Besides the conventional "CAD simulation path" (Fig. 6.2), this work also pursues the "experimental circuit validation path," which takes advantage of the experimental results to benchmark the accuracy of the proposed CAD framework. In terms of the static characteristics, excellent agreement is obtained in the static characteristics of the inverter and ALU at HT, as shown in the < 0.1 V difference in the voltage swing (Fig. 6.4(a)–(b)).

In terms of the dynamic (transient) characteristics, excellent fit between the experimental and simulated t_p of the RO was achieved up to 500 °C (Fig. 6.4(c)). A constant ~ 10 % deviation was found, which could be improved by using future experimental data of higher-stage ROs. For the D flip-flop (DFF), the simulation underestimates the setup time (t_{su}). However, a similar temperature-dependent trend (increase of ~ 8 ns) in t_{su} was found from 25 °C to 500 °C (Fig. 6.4(d)). This is the first study of GaN-based DFF up to 500 °C.

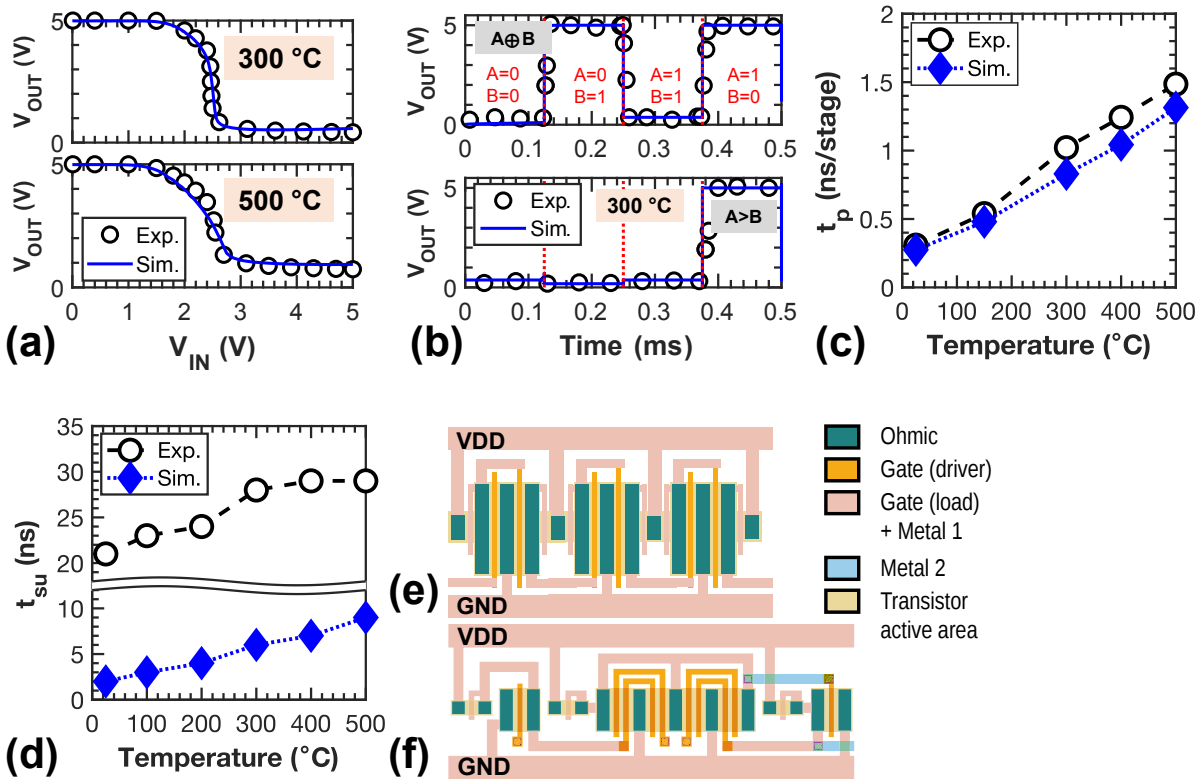


Figure 6.4: Convergence of "CAD simulation path" and "experimental circuit validation path": Experimental results of the circuit proof-of-concept demonstrations are used to compare against the simulations. (a) Inverter voltage transfer curves at 300 °C and 500 °C. (b) Waveform of the ALU at 300 °C. (c) Ring oscillator (RO) (7-stage) propagation delay vs. temperature up to 500 °C. (d) D flip-flop (DFF) setup time *vs.* temperature. This is the first study of GaN-based DFF up to 500 °C. (e)–(f) Layouts of the RO and DFF, respectively. This comparison illustrates the importance of a compact layout and the need for accurate parasitic extraction in the proposed technology. The fabricated circuits are measured up to the rating of the thermal chuck in the particular probe station (two different probe stations with ratings of 300 °C and 500 °C were used). In all circuits, $V_{DD} = 5$ V and no V_{SS}.

Table 6.2: Benchmarking of HT E-Mode GaN HEMTs and their models.

Feature \ Publication (Year)	[23] (2007)	[155] (2002)	[108] (2023)	[153] (2015)	[156] (2020)	This Work [148] (2023)
Transistor type	F-plasma	MIS		p-GaN-gate		p-GaN-gate
Highest temp. (°C)	375	250	400	420	175	500
Compact modeling	–	–	–	–	✓	✓

A major reason for the difference in deviations (absolute values) of t_p and t_{su} is layout parasitics, given that the fabricated RO has a significantly more compact layout than that of the DFF (Fig. 6.4(e)–(f)). Therefore, the inclusion of layout parastiics (in future work) would be highly desired to improve the accuracy of the simulation framework.

Furthermore, the simulation study confirms that, at HT, the increase in t_p and t_{su} is attributed to the lower $I_{D,max}$ and higher R_{ON} in the E-mode transistor, as predicted by circuit theory. The lower $I_{D,max}$ and higher R_{ON} at HT is commonly seen in HEMTs because of degradation in mobility (mainly, polar optical phonon scattering) [154]. While the mobility degradation is unavoidable, one way to ensure high t_p and t_{su} (hence high-speed circuits) is to ensure high $I_{D,max}$ and low R_{ON} at room temperature. Methods include, using an epitxial structure with higher charge density (while not sacrificing E-mode operation), and use of short-channel transistors.

6.5 Benchmarking and Conclusion

To the best of the authors' knowledge, the proposed technology advances the frontier of HT electronics. E-mode GaN transistors were characterized and modeled up to 500 °C, which is the highest temperature for an E-mode transistor (benchmarking in Table 6.2). Indeed, from a device design/structure point-of-view, the p-GaN-gate HEMT is expected to be the most robust at high temperatures ($\geq$ 500 °C). Furthermore, these experimental advances are supported by, and have strengthened the CAD framework for HT technology (benchmarking in Table 6.3): (1) the highest temperature (and widest temperature range) achieved by an experimentally verified CAD framework for GaN technology; (2) simultaneous verification and tuning of the models of two types of

Table 6.3: Benchmarking of recently published HT GaN circuit simulations.

Feature \ Publication (Year)	[22] (2021)	[151] (2021)	[157] (2022)	[158] (2022)	[143] (2017)	This Work [148] (2023)
Wafer	GaN-on-Sapphire	GaN-on-Si	GaN-on-SiC	GaN-on-SiC	SiC	GaN-on-Si
Technology	D-mode (HEMT)	Complementary (p-GaN-gate HEMT + p-FET)	D-mode (HEMT)	D-mode (HEMT)	D-mode RTL (JFET)	E/D-mode (p-GaN-gate HEMT + HEMT)
Integration	3D Bonding	Monolithic	Monolithic	PCB	Monolithic	Monolithic
Highest temp. (°C)	300	300	160, 400, 550	220	961	500
V_{DD} (V)	0	5	14	20	27	5
V_{SS} (V)	−12	No V_{SS}	−14	N.A.	−27	No V_{SS}
Circuit experiment	Oscillator at 1 GHz	–	NAND/NOR, DFF, Voltage ref.	Transmitter at 2 GHz	RO, NOT, NOR, NAND, XOR	ALU
Circuit simulation	(same as above)	RO, SRAM	Passive components	(same as above)	–	ALU, RO, DFF
Circuit sim. verified by exp.	✓	–	–	✓	–	✓

transistors (E-mode and D-mode) using > 6 temperature-dependent parameters in the HT-enhanced MVSG; and (3) verification of CAD framework by ICs of > 10 transistors.

It would be insightful to compare the proposed GaN HT technology (and simulation framework) with SiC, which has been in research and development for a long time [159–164]. Taking the example of [161], the transistor type is SiC junction FET (JFET). The highest temperature is 961 °C, and the digital circuits demonstrated are RO, NOT, NOR, NAND, XOR. However, due to the use of D-mode RTL as the circuit configuration, the rail voltages are $V_{DD}/V_{SS} = 27/-27$ V. A high V_{DD} is required for high noise margins, while the use of V_{SS} is necessary because the transistors are D-mode. As compared to this, the proposed HT technology (and simulation framework) uses $V_{DD} = 5$ V (because of high mobility and current, leading to sufficient noise margin even at 5 V) and no V_{SS} (presence of E-mode transistor which could turn off at $V_{GS} = 0$ V).

This work lays the technology roadmap of the proposed HT GaN technology and takes concrete steps towards the realization of a HT MPU and its DTCO. As part of future research, the proposed roadmap will be extended to HT (> 300 °C) analog mixed-signal and power ICs. In the broader context, this work offers insights for the scaling-up of nascent semiconductor technologies (as exemplified by the proposed technology) to deliver practical microsystems.

Chapter 7

Conclusion and Future Work

7.1 Summary of the Thesis

This thesis seeks to advance electronics based on the p-GaN platform, specifically, to advance complementary GaN transistors, as well as GaN n-FET-based DTCO. To this end, the complementary approaches of experiment and simulation are adopted. At the device-level, the steps involved are the design (and optimization) of novel transistor architectures for both the p-FET and n-FET, the demonstration of new process steps (and their integration in the baseline process flows), the optimization of (baseline) process flow, microscopy (to analyze the device architecture and the material properties), and transistor measurement. Furthermore, the work seeks to translate the impact from the device-level to the circuit-level. This is done through compact modeling, and then simulation/validation at the circuit-level.

The key contributions of this thesis are presented in Fig. 7.1, involving high performance complementary GaN transistors, high performance Si-CMOS-compatible p-FETs, understanding the unique characteristics of p-FETs, a high temperature simulation framework for n-FETs, and analyzing the high temperature performance of p-FETs and n-FETs. Specifically, the contributions of each chapter are presented as follows. The benchmarking of relevant works is conducted to the best of the author's knowledge.

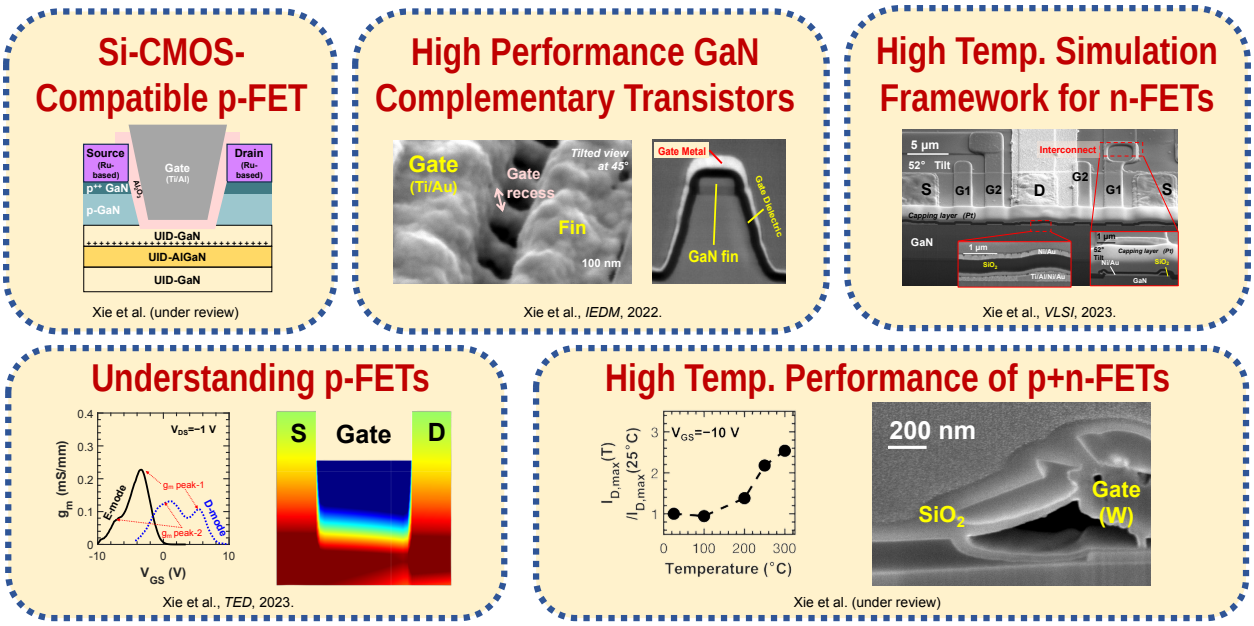


Figure 7.1: Key contributions of this thesis.

Chapter 1 "Introduction" presents an overview of the existing work in GaN electronics based on p-GaN platforms, with an emphasis of two emerging areas of research, namely GaN-CMOS technology and the high temperature GaN electronics. Early experiments have indicated the feasibility of the GaN-CMOS concept. Based on this foundation, GaN-CMOS technology needs to advance to the next-level for greater impact and potential commercialization. Therefore, an application-driven perspective should be adopted in the research of next-generation GaN-CMOS technology. While early experiments are mostly proof-of-concept and perhaps curiosity-driven, Chapter 1 examines the requirements of a practical GaN-CMOS technology (listed in Fig. 1.3), and proposes how these could be addressed. Furthermore, this chapter eludicates the need for a robust simulation framework for GaN ICs (Fig. 6.2) through the example of GaN HT electronics (n-FET-based). This simulation framework is an improvement over the previous "three-step methodology" used for performance projection of novel GaN transistors, because it involves the circuit validation section.

Chapter 2 "Highly Scaled GaN Complementary Technology" reports the demonstration of state-of-the-art complementary GaN transistors based on a GaN-on-Si platform (GaN-CMOS platform). A central theme of this chapter is exploring the scaling limits of novel complementary GaN

transistors, including the p-channel FinFET (scaling in both the channel length direction and the fin width direction), as well as the n-channel p-GaN-gate HEMT (scaling of gate length). A novel gate structure for scaled p-GaN-gate HEMTs was proposed, through the use of refractory metal gate (to withstand annealing in the ohmic-last process), and top metal layers to ensure higher conductivity and masking for the gate etch. Furthermore, the proposed scaled p-GaN-HEMT was fabricated on two epitaxial structures, namely the GaN-CMOS platform (Epi-1) and a conventional p-GaN platform (Epi-2). In both p-FETs and n-FETs, the scaling trends were analyzed. In terms of the benchmarking, the p-FET and n-FET each achieve state-of-the-art performance in their respective categories (based on their conventional benchmarking metrics), and collectively, they deliver a state-of-the-art GaN complementary technology. An ICP-RIE GaN/AlGaN selective etch was developed and would be useful for improved fabrication in the future GaN-CMOS platform.

Chapter 3 "Si-CMOS-Compatible GaN p-FET" addresses the Si-CMOS-compatibility of the p-FET, which is the bottleneck in terms of Si-CMOS-compatibility of the proposed GaN-CMOS technology. The use of Ru-based S/D contacts was demonstrated. These contacts were studied through advanced microscopy (revealing that after annealing, Ru crystal was well-aligned with the p-GaN crystal) and TLM measurements (optimization of annealing temperature). Furthermore, these novel contacts were integrated into the self-aligned p-FET architecture. A novel gate recess technology was proposed to achieve E-mode p-FETs. The p-FETs (first demonstration on MOCVD p-GaN epitaxy) with Ru-based S/D achieve competitive performance among III-N p-FETs, therefore reflecting the potential of the proposed approach to advance the commercialization of p-FETs, without much sacrifice to the transistor performance.

Chapter 4 "Unique Design Space of GaN p-FETs" studies the design space of p-FETs through two parameters unique to the p-FET, namely the gate recess and p-doping profile in p-GaN. While proof-of-concept demonstrations of p-FETs are exciting showcases of the potential of GaN-CMOS, it is equally important to investigate their operation mechanisms and the impact of key design parameters, so as to understand the design space of these emerging transistors. The impact of gate recess depth on the transfer characteristics (E/D-mode, and g_m profile) was studied through

TCAD simulation, which verifies the hypothesis of the existence of two sub-channel components. Later experiments verify the predictions of the simulations. Furthermore, the impact of a realistic p-doping profile (as opposed to the idealized uniform doping) was studied and revealed trade-offs in the p-FET characteristics.

Chapter 5 "p-FETs and n-FETs for High Temperature Operation" investigates the HT performance of the p-FET and n-FET. HT characterization was conducted to analyze the trends of p-FETs for HT operation. Material characterization was conducted to offer a new perspective to the explanations. This section, combined with Chapter 4, deepens the understanding of p-FETs based on the GaN-CMOS platform, and offer several lessons for the design of p-FETs. The proposed p-FET achieves the highest $-I_D$ and $-I_D \times L_G$ at HT, among the p-FETs whose performances at HT are reported. Furthermore, the characterizations of n-FETs *vs.* temperature and after exposure to harsh environment were briefly discussed. The concept of a p-channel junction FET (JFET) was proposed to achieve HT robust p-FETs, and preliminary process development was conducted for the short-channel p-n junction gate.

Chapter 6 "Towards DTCO in high temperature GaN-on-Si technology: a CAD framework up to 500 °C" explores the translation of device-level advancements into circuit-level design, as a first step towards the eventual DTCO of GaN technology. GaN HT electronics based on E/D-mode n-FETs is chosen as a case study. A key challenge was the modeling of the E-mode n-FET (p-GaN-gate HEMT, modified for HT robustness), which is considerably lacking in the literature compared to D-mode n-FETs (conventional HEMTs). This work achieves the highest temperature characterized and modeled of an E-mode GaN transistor. The simulation framework achieves the highest temperature (and widest temperature range) achieved by an experimentally verified CAD framework for GaN technology.

7.2 Future Work

7.2.1 Advancing GaN p-FETs and GaN-CMOS

While GaN-CMOS technology encompasses both n-FETs and p-FETs, the majority of research in the literature have focused on the p-FET, because it is much less mature than the n-FET. This thesis has sought to adopt a more balanced view, by advancing *both* p-FET and n-FET on the GaN-CMOS platform, and demonstrating novel p-FETs which are capable of being eventually integrated on the GaN-CMOS platform.

As mentioned in Chapter 2.5, from a survey of GaN p-FETs, it appears that fundamental advancements need to originate from the material epitaxy and the transistor architecture levels (as opposed to further optimizations of the existing process flows). In terms of material epitaxy, the charge density and mobility of holes need to be increased. Several studies on the origins of the (low) hole mobility (and the mechanisms for scattering) have been conducted [165]. A possible approach is to engineer the strain the epitaxy [166, 167].

There are two aspects to charge density in the p-channel, namely the charge density for bulk p-channel, and the charge density in the 2DHG. For the charge density in the bulk p-GaN, for MOCVD grown p-GaN, it is limited by: (1) the doping limit of Mg in GaN [68], after which the compensation effect steps in; (2) the high activation energy of Mg and the passivation of Mg (Mg-H complex). Mg already has the shallowest acceptor level among acceptors of GaN (as compared to Ca, for instance). Addressing these problems will not only improve p-FETs, but also a wide variety of other GaN devices, including LEDs. Another approach is to add a polarization layer on the p-channel, e.g., AlN (using ALD), which would give more flexibility in device fabrication. Other methods maybe used to increase total charge in the channel, for example, the use of thick p-GaN (whose growth has become more mature to ~ 1 μm), which would necessitate the use of a tall fin architecture to exert effective gate control.

The carrier confinement and gate control in p-FETs needs to be improved, especially for HT

operation. To this end, existing FinFETs could be adopted, but with much improved MIS interfaces. Gate-all-around / nanowire structures could be adopted [168], assuming a suitable sacrificial layer could be found for III-N. Back-gate using the 2DEG underneath the AlGaN (in p-GaN/AlGaN/GaN) could be used [169, 170].

The improvement in carrier confinement could also originate from modifications to the epitaxy. This would be especially relevant if the planar transistor architecture were to be preserved. For example, concepts similar to what is known as a "back barrier" in AlGaN/GaN HEMTs [171, 172] or a "double heterostructure" [173] could be implemented (except that for the p-FET, it would be a top barrier to GaN/AlGaN).

Besides the conventional recessed-gate FETs, novel devices could be explored on the GaN-CMOS platform, including memory devices [174, 175], tunnel FETs [124] and complementary FETs. Similar ideas have been demonstrated in other material systems [50, 176]. Having said that, their value proposition for GaN-CMOS, and conversely, the suitability of GaN for these applications, have yet to be examined.

Alternative substrates such as the engineered substrate [177–179], silicon-on-insulator (SOI) substrate [180], and AlN substrate [181, 182], which have been adopted in recent demonstrations of RF and power transistors, could be used to grow p-GaN epitaxy [177–180]. These substrates each offer various benefits. With the emerging performance of N-polar GaN/AlGaN HEMTs, N-polar AlGaN/GaN p-FETs could be explored, though several challenges remain, such as the formation of ohmic contacts.

7.2.2 Circuit-level prototyping of GaN-CMOS

GaN-CMOS is an advancement at the device (transistor)-level which has the potential to open up tremendous opportunities at the circuit-level. One could immediately think of digital circuits, where GaN-CMOS could replace the existing n-FET-only circuits to reduce static power dissipation. In RF, applications like the compensation of capacitance to reduce AM/PM distortion could be explored. In power electronics, GaN p-FETs could be used for high-side switching. GaN-

CMOS inverter could be used in Class D power amplifiers. The prototyping of some of these circuits would not just serve as proof-of-concept demonstrations. They would allow for a deeper understanding of the device-circuit interactions in different applications and lead to further improvements in the complementary GaN transistors.

7.2.3 Enhancing the Simulation Framework

In order to realize the application proposed in Chapter 7.2.2, a robust device-to-circuit-level simulation framework would be necessary. A major area where the current simulation framework could be enhanced (or expanded) is in GaN-CMOS. Comparing GaN n-FET-only technology and GaN-CMOS technology, there are pros and cons of each, in terms of technological maturity, temperature dependency, static power dissipation etc. With the advancement of GaN-CMOS technology, the prospects of GaN-CMOS technology for many circuit applications should not be underestimated.

At the heart of the device-to-circuit-level simulation framework is a robust compact model. While the general principles of the MVSG model (e.g. carrier injection from the virtual source, charge formulation in the gate region) are applicable for p-FETs, there may need to be some modifications. For example, one would need to take into account the bulk channels in the access regions, therefore the R_{sh} is not constant in the entire channel. Other unique effects like the "field-induced acceptor ionization" would need to be modeled. The prerequisite is extensive characterization of the p-FET.

From the circuit perspective, GaN-CMOS technology (currently in device-level research) would need to evolve to a process design kit (PDK). There are several hurdles to be overcome, and the technology needs to be transferred to a commercial foundry for a stable process. After a stable process, the parasitics in the FEOL (especially p-FET) and BEOL (of the GaN-CMOS platform) need to be carefully calculated. Sufficient demand for GaN-CMOS from the circuit-level would give a push to the advancement of the PDK. This would allow GaN-CMOS technology to serve a wide variety of applications (RF, power, mixed-signal etc.) and make this technology truly beneficial for the society.

Appendix A

Process Flows

GaN p-FET
(Baseline Flow for Planar Transistor)

Process and process number	Process steps	Tool(s)
1. Wafer dicing	Wafer dicing	• DAD-3240
2. Wafer cleaning	Clean wafer as described in the first cleaning step	• Solvent-Clean-U06
3. Piranha clean	Piranha (H_2SO_4:H_2O_2 3:1) dip 15 min.	• Acid-Etch-General-U10
4. Ohmic contact	Lithography (Optical lithography or electron beam lithography)	• HMDS-Yes-U10 • Spinner-Resist-U12 • Spinner-PMGI-U12 • Spinner-EBL • DirectWrite-MLA150 • EBL
	Ni/Au (lift-off) 30 / 50 nm <u>Note:</u> If optical resist is used, do oxide strip using BOE (7:1) for 2 min. immediately before loading the sample in the deposition chamber. If electron beam resist is used, do the oxide strip step immediately before the spin coating of the resist, and after development of the resist, immediately load the sample in the deposition chamber.	• EBeamAU • EBeam-Temescal-LL • EBeam-AJA • Sputter-AJA-ChamberLoad
	Annealing in N_2/O_2 ambient	• B1 Tube • RTA-1300C-ASOne150-5Gas
5. Mesa etch	Lithography	• HMDS-Yes-U10 • Spinner-Resist-U12 • DirectWrite-MLA150
	GaN etch (photoresist mask)	• RIE-Cl2-SAMCO-200iP • RIE-Mixed-SAMCO-230iP • Oxford-100
	Removal of photoresist mask O_2 plasma (asher)	• Asher-Barrel-Thierry

Process and process number	Process steps	Tool(s)
6. Gate recess	Lithography (for non-self-aligned gate recess only)	• HMDS-Yes-U10 • Spinner-Resist-U12 • Spinner-PMGI-U12 • Spinner-EBL • DirectWrite-MLA150 • EBL
	GaN etch	• RIE-Cl2-SAMCO-200iP • RIE-Mixed-SAMCO-230iP • Oxford-100
	Removal of photoresist mask (if used) O_2 plasma (asher)	• Asher-Barrel-Thierry
7. Post-gate recess treatment	Hot (75 ºC) TMAH	• Acid-Etch-General-U10
	Annealing in N_2 ambient at 500 ºC	• B1 Tube
8. Gate dielectric	SiO_2 ALD Chamber at 250 °C. TDMAS precursor at room temperature. Pulse widths and spacing between the pulses: for Si precursor, pulse time is 2 s; spacing purge time is 4 s. For O_2, pulse time is 30 s (plasma power on time 27 s, the flow stabilization time is 3 s) spacing purge time is 4 s. Precursor and O_2 flow, O_2 plasma power: carrier gas flow with precursor is 120 sccm, plasma gas flow is 100 sccm; the plasma power is 2800 W.	• ALD (CMDIS, Rensselaer Polytechnic Institute) Acknowledgement: Dr. Xiaohong An Mr. Bryant C. Colwill
9. Gate metallization	Lithography	• HMDS-Yes-U10 • Spinner-Resist-U12 • Spinner-PMGI-U12 • Spinner-EBL • DirectWrite-MLA150 • EBL
	Gate metal (lift-off) e.g. Ti/Au	• EBeamAU • EBeam-Temescal-LL • EBeam-AJA • Sputter-AJA-ChamberLoad

For Ru contacts:
RF magnetron sputtering using Sputter-AJA-ChamberLoad
Ru target, deposition rate = 1 Å/s, RF power ~ 160 W, Ar flow at 12 sccm
Anneal in Tube-OxAnneal-Regular (Expertech CTR-200), N_2/O_2 (1:2), 500 °C

To deposit RuO_x by RF reactive magnetron sputtering:
Ru target, O_2/Ar flow=4/8 sccm

GaN p-FET
(GaN Self-Aligned p-FinFET)

Process and process number	Process steps	Tool(s)
1. Wafer dicing	Wafer dicing	• DAD-3240
2. Wafer cleaning	Clean wafer as described in the first cleaning step	• Solvent-Clean-U06
3. Piranha clean	Piranha (H_2SO_4:H_2O_2 3:1) dip 15 min.	• Acid-Etch-General-U10
4. Ohmic contact	Lithography (Optical lithography or electron beam lithography)	• HMDS-Yes-U10 • Spinner-Resist-U12 • Spinner-PMGI-U12 • Spinner-EBL • DirectWrite-MLA150 • EBL
	Ni/Au/Ni (lift-off) 30/50/30 nm	• EBeamAU • EBeam-Temescal-LL • EBeam-AJA • Sputter-AJA-ChamberLoad
	Annealing in N_2/O_2 ambient 550 ºC, N_2/O_2 (1:1), 45 min.	• B1 Tube
5. Mesa and fin etch	Lithography (fin) • Surpass 3000 as adhesion promoter • HSQ (4% or 6 %), 750 rpm (6 sec.), 3000 rpm (60 sec.) • EBL • Develop in TMAH (25 %), room temperature, 85 sec.	• Spinner-EBL • EBL
	Lithography (mesa)	• HMDS-Yes-U10 • Spinner-Resist-U12 • DirectWrite-MLA150
	GaN etch Cl_2/BCl_3 (3:1), 0.6 Pa Etch rate of ~1 nm/sec.	• RIE-Cl2-SAMCO-200iP • RIE-Mixed-SAMCO-230iP • Oxford-100
	Removal of photoresist mask O_2 plasma (asher)	• Asher-Barrel-Thierry
	BOE 1-2 min. to remove HSQ (SiO_2)	• Acid-Etch-General-U10
6. Gate recess	GaN etch Cl_2/BCl_3 (3:1), 0.6 Pa Etch rate of ~1 nm/sec.	• RIE-Cl2-SAMCO-200iP • RIE-Mixed-SAMCO-230iP • Oxford-100
7. Post-gate recess treatment	Hot (75 ºC) TMAH, 5 min.	• Acid-Etch-General-U10

Process and process number	**Process steps**	**Tool(s)**
	Annealing in N_2 ambient 500 ºC, >30 min.	• B1 Tube
8. Gate dielectric	SiO_2 by TDMAS + O_2 plasma at 250 ºC	• ALD
9. Gate metallization	Lithography	• HMDS-Yes-U10 • Spinner-Resist-U12 • Spinner-PMGI-U12 • Spinner-EBL • DirectWrite-MLA150 • EBL
	Gate metal (sputtering, lift-off) e.g. Ti/Au	• Sputter-AJA-ChamberLoad

GaN n-FET

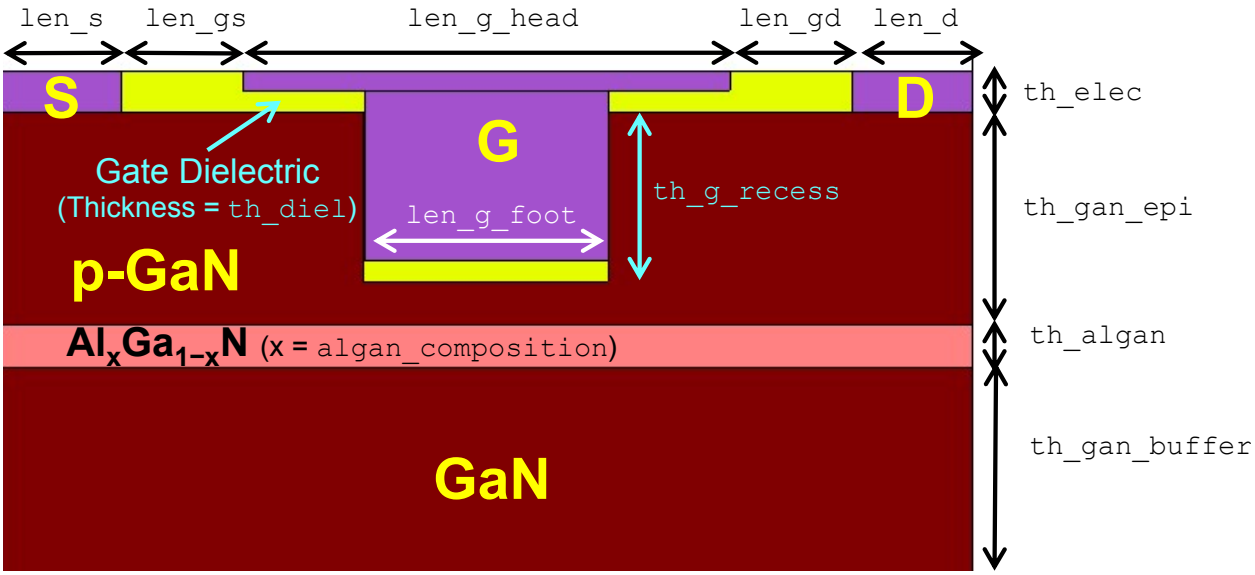
(p-GaN-Gate HEMT with Self-Aligned Metal/p-GaN Gate)

Process and process number	**Process steps**	**Tool(s)**
10. Wafer dicing	Wafer dicing	• DAD-3240
11. Wafer cleaning	Clean wafer as described in the first cleaning step	• Solvent-Clean-U06
12. Piranha clean	Piranha (H_2SO_4:H_2O_2 3:1) dip 15 min.	• Acid-Etch-General-U10
13. Gate Metallization	W (100 – 200 nm) (blanket sputtering without lift-off)	• Sputter-AJA-LL • Sputter-AJA-ChamberLoad
14.	Lithography (Electron beam lithography) *Note: Alignment markers may be defined in this step.*	• Spinner-EBL • EBL
15.	Ni/Au/Ni (30/120/80 nm) Lift-off	• EBeamAU • EBeam-Temescal-LL
16. Gate etch	W etch SF_6/O_2	• Oxford-100 • RIE-Mixed-SAMCO-230iP
17.	GaN etch (selective over AlGaN) BCl_3/SF_6 *Note: While there is considerable selectivity in AlGaN over GaN, typically a few calibration runs are conducted immediately before the actual run. In these calibration runs, AFM (for step height of p-GaN island) will be done and ohmic contacts (to 2DEG, without p-GaN island) will be measured.*	• Oxford-100 • RIE-Mixed-SAMCO-230iP
18. Ohmic contact	Lithography (Optical lithography or electron beam lithography)	• HMDS-Yes-U10 • Spinner-Resist-U12 • Spinner-PMGI-U12 • Spinner-EBL • DirectWrite-MLA150 • EBL
19.	Ti/Al/Ni/Au (20/100/25/50 nm) Lift-off	• EBeamAU • EBeam-Temescal-LL
20.	Alloying of metal stack 800 ºC, N_2 ambient, 30 s	• RTA-1100C-ASMicro • RTA-1300C-ASOne150-5Gas
21. Mesa etch	Lithography	• HMDS-Yes-U10 • Spinner-Resist-U12 • DirectWrite-MLA150

Process and process number	**Process steps**	**Tool(s)**
22.	GaN etch (photoresist mask)	• RIE-Cl2-SAMCO-200iP • RIE-Mixed-SAMCO-230iP • Oxford-100
23.	Removal of photoresist mask O_2 plasma (asher)	• Asher-Barrel-Thierry • Asher-Chuck-ESI
24. Probe pad	Lithography	• HMDS-Yes-U10 • Spinner-Resist-U12 • DirectWrite-MLA150
25.	Ti/Au or Ni/Au (30/150 nm) Lift-off	• EBeamAU • EBeam-Temescal-LL

Appendix B

Simulation Deck for p-FET



doping_algan	Doping of AlGaN, e.g. Si background doping
doping_gan_buffer	Doping of GaN buffer, e.g. Si background doping

Figure B.1: Device structure and key parameters of the p-FET in the TCAD simulation setup.

```
set dir_str = "device_str"
set str_name_basic = "pmos_tgate_recess_$'th_g_recess'um"

set len_diel = $th_diel
set th_g_head = $th_elec
set th_g_foot = $th_g_recess - $th_diel

#set voltage sweep variables

set sweep_type = "VG"
set dir_init_str = "output_init_str"
set dir_VG = "output_VG"
set dir_VG_str = "output_VG_str"
set dir_VD = "output_VD"
set dir_VD_str = "output_VD_str"


#VG sweep
set vd_biaspt_initial = -1
set vd_biaspt_final = -1
set vd_biaspt_step = -1
set vd_biaspt_nsteps = (floor(($vd_biaspt_final-$vd_biaspt_initial)/
   $vd_biaspt_step)+1)
set vg_sweep_initial = 5
set vg_sweep_final = -10
set vg_sweep_step = -.1
set vg_sweep_nsteps = (floor(($vg_sweep_final-$vg_sweep_initial)/
   $vg_sweep_step)+1)

#VD sweep
set vg_biaspt_initial = -5
set vg_biaspt_final = -5
set vg_biaspt_step = -1
set vg_biaspt_nsteps = (floor(($vg_biaspt_final-$vg_biaspt_initial)/
   $vg_biaspt_step)+1)
set vd_sweep_initial = 0
set vd_sweep_final = -10
set vd_sweep_step = -.1
set vd_sweep_nsteps = (floor(($vd_sweep_final-$vd_sweep_initial)/
   $vd_sweep_step)+1)


#set x (length) coordinates
set x_device_1 = 0
set x_s_1 = $x_device_1
set x_s_2 = $x_s_1 + $len_s
set x_g_head_1 = $x_s_2 + $len_gs
```

```
set x_diel_1 = $x_g_head_1 + .5*($len_g_head - $len_g_foot) -
   $len_diel
set x_g_foot_1 = $x_g_head_1 + .5*($len_g_head - $len_g_foot)
set x_g_foot_2 = $x_g_foot_1 + $len_g_foot
set x_diel_2 = $x_g_foot_2 + $len_diel
set x_g_head_2 = $x_g_head_1 + $len_g_head
set x_d_1 = $x_g_head_2 + $len_gd
set x_d_2 = $x_d_1 + $len_d
set x_device_2 = $x_d_2

#set z (depth) coordinates
set z_gan_epi_1 = 0
set z_gan_epi_2 = $z_gan_epi_1 + $th_gan_epi
set z_algan_1 = $z_gan_epi_2
set z_algan_2 = $z_algan_1 + $th_algan
set z_gan_buffer_1 = $z_algan_2
set z_gan_buffer_2 = $z_gan_buffer_1 + $th_gan_buffer
set z_diel_1 = $z_gan_epi_1 - $th_diel
set z_diel_2 = $z_gan_epi_1 + $th_g_recess
set z_g_head_2 = $z_gan_epi_1 - $th_diel
set z_g_head_1 = $z_g_head_2 - $th_elec
set z_g_foot_1 = $z_g_head_2
set z_g_foot_2 = $z_diel_2 - $th_diel
set z_s_1 = $z_gan_epi_1 - $th_elec
set z_s_2 = $z_gan_epi_1
set z_d_1 = $z_gan_epi_1 - $th_elec
set z_d_2 = $z_gan_epi_1
set z_passivation_1 = $z_g_head_1
set z_passivation_2 = $z_diel_1

go atlas

mesh width=1

# x axis meshing
x.mesh l=$x_device_1 s=($len_s/3)
x.mesh l=$x_s_2 s=($len_gs/5)
x.mesh l=($x_g_head_1-.1) s=($len_g_foot/30)
x.mesh l=$x_g_head_1 s=($len_g_foot/25)
x.mesh l=$x_diel_1 s=($len_diel/6)
x.mesh l=$x_g_foot_1 s=($len_g_foot/25)
x.mesh l=$x_g_foot_2 s=($len_g_foot/25)
x.mesh l=$x_diel_2 s=($len_diel/6)
x.mesh l=$x_g_head_2 s=($len_g_foot/25)
x.mesh l=($x_g_head_2+.1) s=($len_g_foot/30)
x.mesh l=$x_d_1 s=($len_gs/5)
x.mesh l=$x_device_2 s=($len_d/3)
```

```
90
91 # y axis meshing
92 y.mesh l=$z_diel_1 s=($th_diel/6)
93 y.mesh l=$z_g_head_1 s=($th_g_head/5)
94 y.mesh l=$z_gan_epi_1 s=($th_diel/6)
95 y.mesh l=$z_g_foot_2 s=($th_diel/6)
96 y.mesh l=$z_diel_2 s=($th_diel/6)
97 y.mesh l=$z_gan_epi_2 s=($th_diel/5)
98 y.mesh l=$z_algan_2 s=($th_diel/5)
99 y.mesh l=$z_gan_buffer_2 s=($th_gan_buffer/4)
100
101
102 region num=1 x.min=$x_device_1 x.max=$x_device_2 y.min=$z_gan_epi_1
      y.max=$z_gan_epi_2 material=GaN
103 region num=2 x.min=$x_device_1 x.max=$x_device_2 y.min=$z_algan_1
      y.max=$z_algan_2 material=AlGaN x.composition=$algan_composition
      donors=$doping_algan
104 region num=3 x.min=$x_device_1 x.max=$x_device_2 y.min=
      $z_gan_buffer_1 y.max=$z_gan_buffer_2 material=GaN donors=
      $doping_gan_buffer
105 region num=4 x.min=$x_diel_1 x.max=$x_diel_2 y.min=$z_gan_epi_1 y.max
      =$z_diel_2 material=Al2O3 insulator
106 region num=5 x.min=$x_device_1 x.max=$x_device_2 y.min=$z_g_head_1
      y.max=$z_gan_epi_1 material=Al2O3 insulator
107 region num=6 x.min=$x_device_1 x.max=$x_device_2 y.min=
      $z_passivation_1 y.max=$z_passivation_2 material=nitride insulator
108 #regions 4-5: gate dielectric; region 6: passivation
109
110 electrode num=1 name=source x.min=$x_s_1 x.max=$x_s_2 y.min=$z_s_1
      y.max=$z_s_2
111 electrode num=2 name=drain x.min=$x_d_1 x.max=$x_d_2 y.min=$z_d_1
      y.max=$z_d_2
112 electrode num=3 name=gate x.min=$x_g_foot_1 x.max=$x_g_foot_2 y.min=
      $z_g_foot_1 y.max=$z_g_foot_2
113 electrode num=4 name=gate x.min=$x_g_head_1 x.max=$x_g_head_2 y.min=
      $z_g_head_1 y.max=$z_g_head_2
114 electrode num=5 substrate
115
116 #doping for GaN epi
117 doping acceptors concentration=2e19 uniform \
118   x.min=$x_device_1 x.max=$x_device_2 y.min=$z_gan_epi_1 y.max=(
        $z_gan_epi_1+.05)
119 doping acceptors concentration=5e18 uniform \
120   x.min=$x_device_1 x.max=$x_device_2 y.min=($z_gan_epi_1+.05) y.max=
        $z_gan_epi_2
121
122 save outfile="$'dir_str'/$'str_name_basic'.str"
```

```
123
124 set str_name = "$'str_name_basic'"
125
126 ### To solve the model ###
127
128 go atlas
129
130 mesh infile="$'dir_str'/$'str_name_basic'.str" width=1
131
132 contact name=gate workfun=4.5
133 contact name=source workfun=8
134 contact name=drain workfun=8
135
136 models print srh auger fermi
137 models incomplete
138
139 mobility region=1 fldmob.p mup=20 vsatp=1e5 betap=.725
140 mobility region=3 albrct.n
141 material material=gan eab=.24
142 material material=Al2O3 insulator eg300=8.9 affinity=2
143
144
145 models polarization calc.strain polar.scale=.75
146
147 output con.band val.band polar.charge band.par qss e.field charge
      h.mobility h.velocity e.mobility e.velocity
148
149
150 method newton itlim=30 trap maxtrap=8 carriers=1 holes
151
152 solve init
153 save outfile="$'output_init_str'/$'str_name'_init.str"
154
155 ### VG Sweep
156 if cond = (@sweep_type = "VG")
157
158 loop steps=$vd_biaspt_nsteps
159 assign name=vd_biaspt n.value=$vd_biaspt_initial delta=
      $vd_biaspt_step
160 set log_filename = "$'dir_VG'/$'str_name'_VD_$'vd_biaspt'
      _VG_sweep.log"
161
162 solve init
163 solve name=drain vstep=(.25*$vd_biaspt) vfinal=$vd_biaspt
164
165 solve vgate=$vg_sweep_initial
166
```

```
log outfile="$'log_filename'"

loop steps=$vg_sweep_nsteps
assign name=vg n.value=$vg_sweep_initial delta=$vg_sweep_step
set vg_outfile_name = "$'dir_VG_str'/$'str_name'_VD_$'vd_biaspt'_VG_$'vg'.str"
solve vgate=$vg outfile="$'vg_outfile_name'" master onefileonly

# to extract the data from .str file
extract init infile="$'dir_VG_str'/$'str_name'_VD_$'vd_biaspt'_VG_$'vg'.str"
extract name="temp" 2d.conc.file impurity="Cond. Current Density" material="GaN" y.min=$z_gan_epi_1 y.max=$z_gan_epi_2 outfile="$'dir_VG_str'/$'str_name'_VD_$'vd_biaspt'_VG_$'vg'_condcurrent.dat"
extract name="temp" 2d.conc.file impurity="Hole Conc" material="GaN" y.min=$z_gan_epi_1 y.max=$z_gan_epi_2 outfile="$'dir_VG_str'/$'str_name'_VD_$'vd_biaspt'_VG_$'vg'_holeconc.dat"

l.end

log off

extract init infile="$'log_filename'"
extract name="IdVg" curve(v."gate", i."drain") outfile="$'dir_VG'/$'str_name'_VD_$'vd_biaspt'_VG_sweep_IDVG.dat"
l.end
#end: loop VD
if.end
#end: if sweep VG

####################
#VD sweep
if cond = (@sweep_type = "VD")

loop steps=$vg_biaspt_nsteps
assign name=vg_biaspt n.value=$vg_biaspt_initial delta=$vg_biaspt_step
set log_filename = "$'dir_VD'/$'str_name'_VG_$'vg_biaspt'_VD_sweep.log"

solve init
solve name=gate vstep=(.125*$vg_biaspt) vfinal=$vg_biaspt

log outfile="$'log_filename'"
solve name=drain vdrain=$vd_sweep_initial vfinal=$vd_sweep_final vstep=$vd_sweep_step

```

```
loop steps=$vd_sweep_nsteps
assign name=vd n.value=$vd_sweep_initial delta=$vd_sweep_step
solve name=drain vfinal=$vd outfile="$'dir_VD'/$'str_name'_VG_$'
   vg_biaspt'_VD_$'vd'.str" master onefileonly
l.end

log off

extract init infile="$'log_filename'"
extract name="IdVd" curve(v."drain", i."drain") outfile="$'dir_VD'/$'
   str_name'_VG_$'vg_biaspt'_VD_sweep_IDVD.dat"
l.end

if.end
#end: if sweep VD
```

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