The Design of
Integrated Distributed Amplifiers

by

Jeffrey Clay McHarg

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INTEGRATED DISTRIBUTED AMPLIFIERS

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Submitted to the Department of Electrical Engineering and Computer Science on January 18, 1980 in partial fulfillment of the requirements for the Degrees of Bachelor of Science in Electrical Engineering and Master of Science in Electrical Engineering and Engineer in Electrical Engineering

ABSTRACT

Computer programs in APL were written to implement microstrip design formulas presented by Wheeler. With the use of these formulas, several different distributed amplifiers were designed for production at IBM, Endicott, NY. Layout of these designs was also undertaken.

At the same time, computer simulation of the various topologies was performed. Results of this circuit analysis indicated proper operation as backed by theory. In specific, the gain-bandwidth product increased as the square of the number of stages, a result not expected for parallel transistors but predicted by distributed amplification theory.

Completed test wafers were tested at Lincoln Laboratory using a mini-computer controlled spectrum analyzer. Four amplifiers were completely characterized; two multiple stage designs and their corresponding single stage amplifiers. An increase in gain-bandwidth product was found. Further, the measured results were close to those predicted by simulation.

Further simulation of the multiple stage results from the single stage results failed, possibly due to phase shift in the single stage measured results introduced by the test fixture.

Thesis Supervisor: Dr. Paul Penfield, Jr.

Title: Professor of Electrical Engineering

TABLE OF CONTENTS

INTRODUCTION

Distributed amplification is a technique for circuit design that yields very high bandwidth systems. Its principles have been fully explained for many years, having been introduced in August, 1948 by Edward L. Ginzton, et al, in an article published in Proceedings of the I.R.E. entitled "Distributed Amplification". At that time, the main purpose of this circuit design technique was to extend the bandwidth of vacuum tube amplifiers into the hundreds of megahertz range.

Although known as a design technique, its popularity was limited, presumably due to the relative inefficiency in terms of gain per vacuum tube, and to the difficulty in designing with it. The advent of transistors and their proportionally higher bandwidth virtually eliminated distributed amplifiers as a design alternative.

Since then, progress in this area has been sporadic, but possible applications at low gigahertz frequencies have led to recent renewed interest in this field. The integration of the entire circuit would allow easier use of distributed amplifiers in many applications.

This, then, is the purpose of this thesis: to develop, model, fabricate, test, and analyze an integrated distributed amplifier. To this end, a quick review of distributed amplification theory will be the first topic addressed. Secondly, the appropriate equations necessary for the

development of transmission line parameters will be presented and discussed.

Having dealt with the needed theory and equation derivation, circuit layout, simulation and fabrication are next explained. Emphasis is placed on the predicted behavior of the finished device in this section.

After this, the testing procedures used and the results obtained are provided. Only a partial presentation will occur within the body of the text, the majority of the results being left for the appendices.

Finally, the results are analyzed, interpreted and compared to those that were predicted earlier in the paper. Final summary and appendices follow this section.

My efforts in this project have met with strong support from all directions, for which I am grateful. In particular, I would like to thank those persons at IBM who helped make this project a success: Andrew Johnson, for suggesting this topic and supervising my work during the first half of my employ at IBM, Richard Moyer, for his supervision and expiditing during the second part of my project, David Grindel, whose help with the technicalities of preparing a chip for production were invaluable, Bart Medvecki, Edward Winter, and Edward Mohring for their time, patience, and speed in pushing to an early completion date.

I would also like to thank those who have supported my efforts at MIT and Lincoln Laboratories: Paul Penfield, Jr., for advice and supervision, Dr. Ron Bauer and Richard

Michalik, for their help in results analysis and the mechanics of testing the finished devices.

DISTRIBUTED AMPLIFICATION THEORY

Formally, a distributed amplifier is a series of gain elements whose inputs are connected to a tapped input delay line, and whose outputs are connected to a tapped output delay line. Each transmission line is terminated in its characteristic impedance to eliminate reflections, and the electrical length between one input and the next is the same as the electrical length from that output to the next, i.e. the delay between input taps is the same as the delay between output taps. These ideas are illustrated in Fig. 2.1.

In more detail, a signal is sent propagating down an input transmission line and is tapped off by the first gain stage. This stage is assumed to have a high input impedance compared to the characteristic impedance of the line, so as not to attenuate the input signal. Thus the signal continues to propagate further and at the same time is amplified through the first stage.

The output of the first stage sends the amplified signal in both directions along the output transmission line. One direction leads to the termination impedance while the other leads to the output of the second gain stage.

Meanwhile, the input signal passes the input to the second stage, is tapped off again and is amplified. If the delays through the two stages are the same and the delays

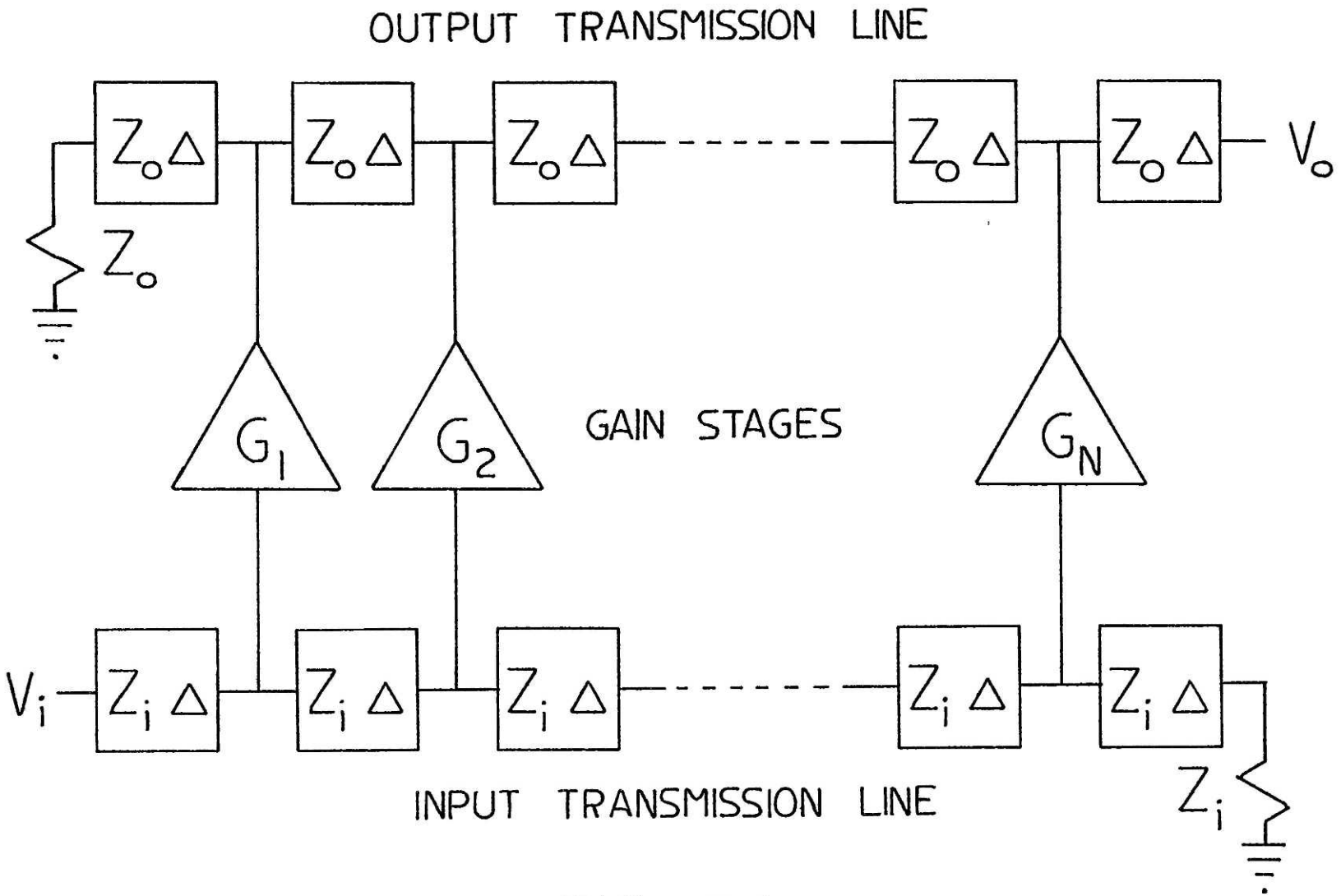

OUTPUT TRANSMISSION LINE
$Z_o\Delta$
$Z_o\Delta$
$Z_o\Delta$
$Z_o\Delta$
$Z_o\Delta$
V_o
Z_o
G_1
G_2
GAIN STAGES
G_N
V_i
$Z_i\Delta$
$Z_i\Delta$
$Z_i\Delta$
$Z_i\Delta$
$Z_i\Delta$
INPUT TRANSMISSION LINE
Z_i

FIG. 2.1

between the input taps and the output taps are the same, the signal from the first stage will arrive at the output of the second stage at the same time as the signal through the second stage. Thus, the forward travelling waves from the two stages will add constructively, whereas the reverse travelling waves will be dissipated in the terminating impedance.

This process is repeated through each stage until the end of the line is reached. At this point, the input signal is terminated in the characteristic impedance of the input transmission line and the signal on the output line is used as the amplifier output.

One important thing to note about this type of amplifier is that there is considerable delay between the input and the output. This makes such circuit practices as feedback useless. Another important point is that the gain stages are effectively connected in parallel instead of cascaded. Thus, the gain of the overall amplifier is the sum of the gains of the individual stages, not their product. This is particularly important when considering the type of gain stage which is to be employed. For example, a gain stage with less than unity power gain may still be used for an overall power gain of greater than one. In a similar vein, the bandwidth of a number of identical stages connected as a distributed amplifier is equal to the bandwidth of an individual stage. But the bandwidth of a number of cascaded stages is less than the

smallest bandwidth of any of its stages.

Due to the design of the distributed amplifier, this last statement can quite often be improved upon. To see this, let us analyze a single stage of this amplifier, including its input and output transmission lines. We will use as a gain element a grounded base transistor as illustrated in Fig. 2.2. Utilizing the hybrid-pi model for the transistor, the incremental circuit becomes that of Fig. 2.3. Note that the generalized transmission lines of Fig. 2.2 have been replaced by their lumped element equivalents in Fig. 2.3. With the circuit drawn in this manner, it becomes evident that the capacitance, C_π, can be considered as an element of the input transmission line. Similarly, the capacitance, C_μ, can be absorbed by the output transmission line model.

This illustrates one of the strengths of the distributed amplifier connection. Namely, any input or output capacitances are decoupled from the rest of the circuit. This also points out the importance of the transmission line links between stages. If, for example, the common base structures are simply paralleled, the overall gain is increased because of the parallel dependent current sources, but the input and output capacitances are increased by the same factor, so the gain-bandwidth product remains effectively unchanged.

Treating C_π as a component in the input delay line, the characteristic impedance of the input line becomes,

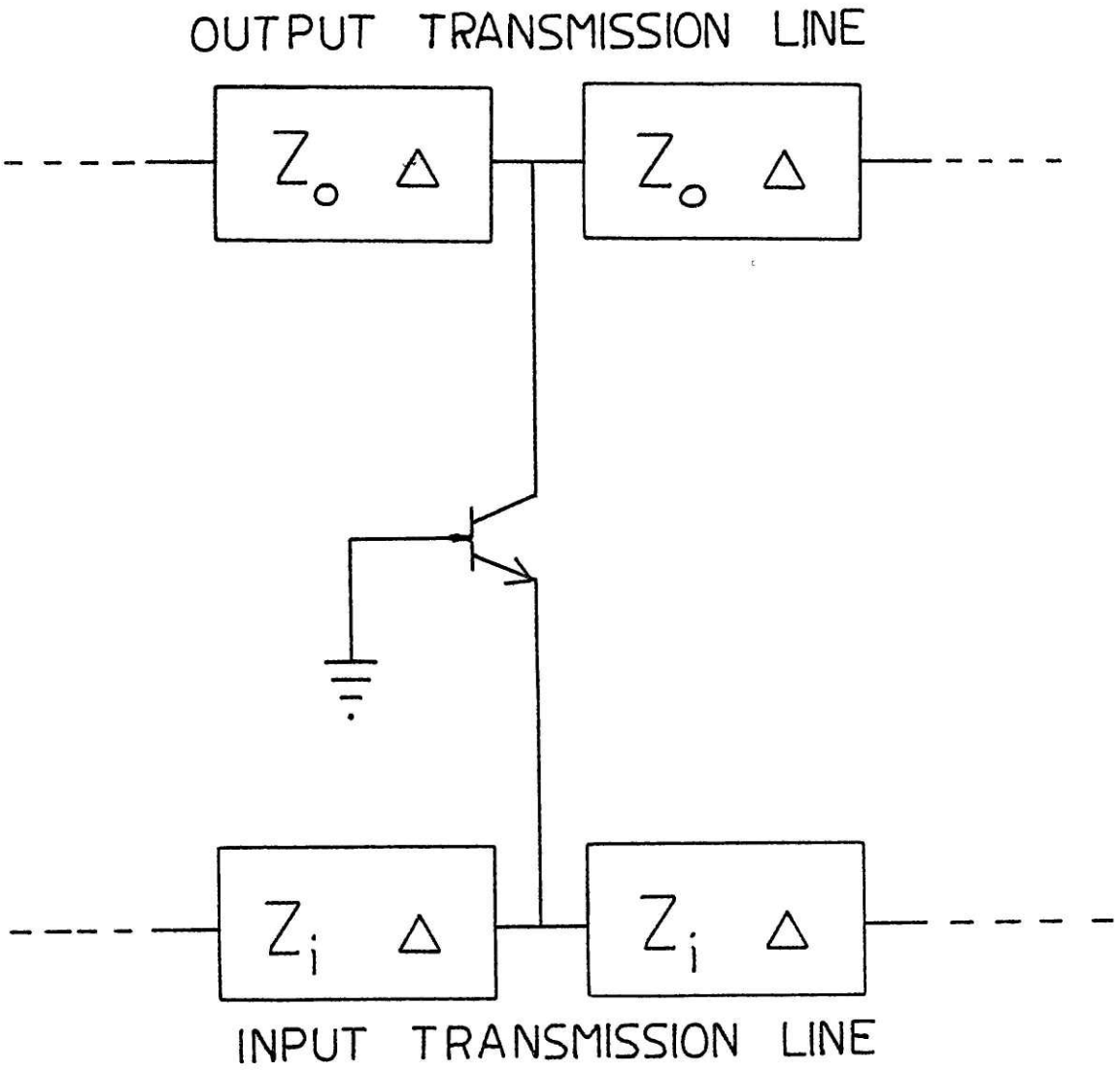

OUTPUT TRANSMISSION LINE
Z_o Δ
Z_o Δ
Z_i Δ
Z_i Δ
INPUT TRANSMISSION LINE

FIG. 2.2

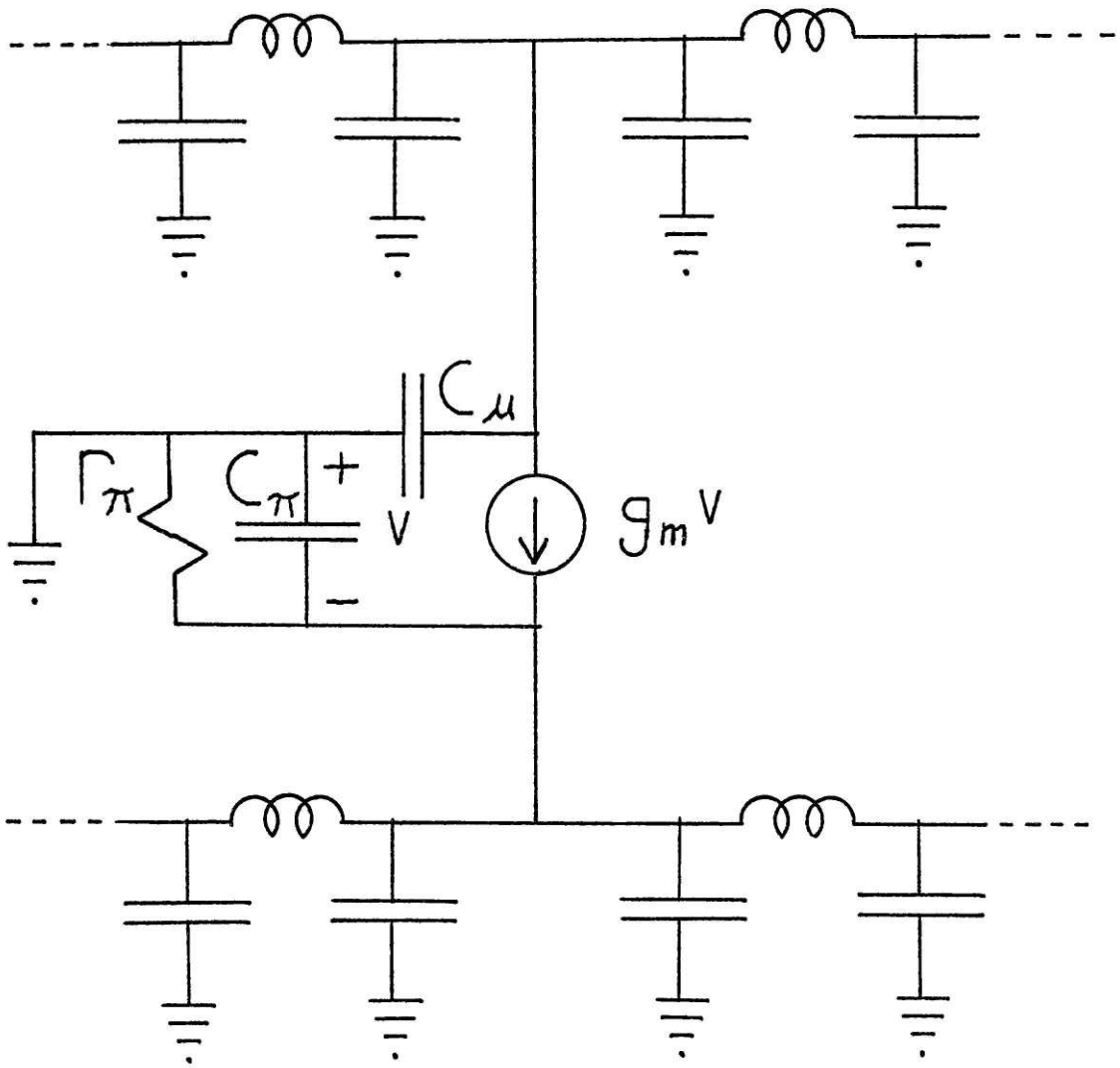


FIG. 2.3

$$Z_i' = Z_i \sqrt{\frac{\Delta}{\Delta + Z_i C_\pi}} \quad ,$$

where Z_i is the input line impedance without C_π, Δ is the delay between stages without C_π, and Z_i' is the line impedance with C_π. A similar equation holds true for the output delay line:

$$Z_o' = Z_o \sqrt{\frac{\Delta}{\Delta + Z_o C_\mu}} \quad ,$$

where Z_o is the output line impedance without C_μ, and Z_o' is the output line impedance with C_μ.

Using these effective line impedances, Fig. 2.3 can be redrawn, yielding the simpler configuration of Fig. 2.4. The gain of this circuit is easily shown to be,

$$G_o = \frac{g_m r_\pi Z_o'}{2(g_m r_\pi + 1)Z_i' + 4r_\pi}$$

$$\cong \frac{g_m Z_o'}{4}$$

where r_π is the incremental input resistance of the transistor, g_m is the incremental transconductance of the transistor, and G_o is the incremental small signal gain, V_o/V_i, of the stage. Note that the effective resistance seen by the output of the transistor is one-half the characteristic impedance of the output delay line, due to the fact that signals must be sent in both directions along the output line.

The overall voltage gain of an N-stage distributed amplifier, G_N, is then,

$$G_N = NG_o \quad .$$

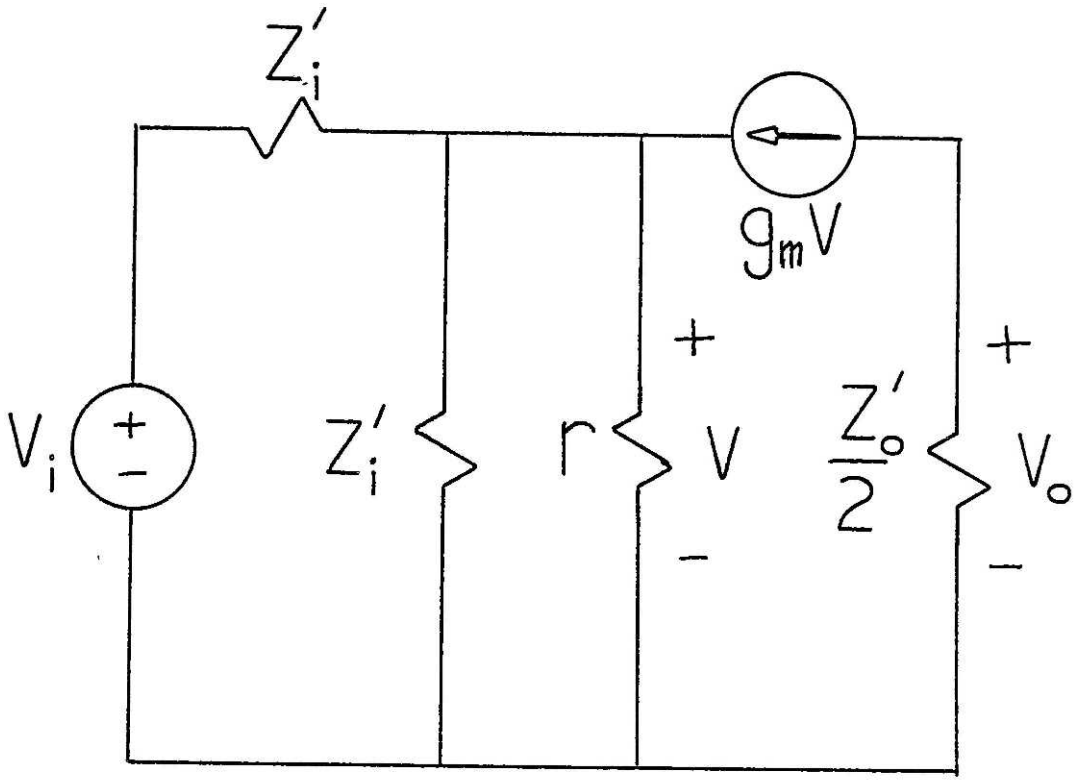


FIG. 2.4

In order to calculate the power gain of the entire circuit, it must be remembered that half of the output power is dissipated in the reverse termination resistor. Keeping this in mind, the power input to the circuit, P_{in}, is,

$$P_{in} = V_i^2/2Z_i' \quad ,$$

and the power at the output, P_o, is,

$$P_o = V_o^2/Z_o' \quad .$$

Thus the total power gain, $G_p = P_o/P_{in}$, is,

$$\begin{aligned} G_p &= 2V_o^2 Z_i'/V_i^2 Z_o' \\ &= 2G_N^2 Z_i'/Z_o' \\ &\cong g_m^2 N^2 Z_o' Z_i'/8 \quad . \end{aligned}$$

As predicted, the total power gain increases as the number of stages increases.

The above results, though derived for a specific gain element, work, at least on a qualitative basis, when applied to a variety of similar circuits. As a simple example, consider replacing the common base stage with a common emitter stage. This is shown in Fig. 2.5, while the appropriate incremental model is shown in Fig. 2.6. As in the case of the common base stage, the capacitance, C_π, can be incorporated into the delay line, but because C_μ is not connected to ground, the same is not true of C_μ and the output delay line. C_μ does create an important effect in this configuration, but discussion of this will

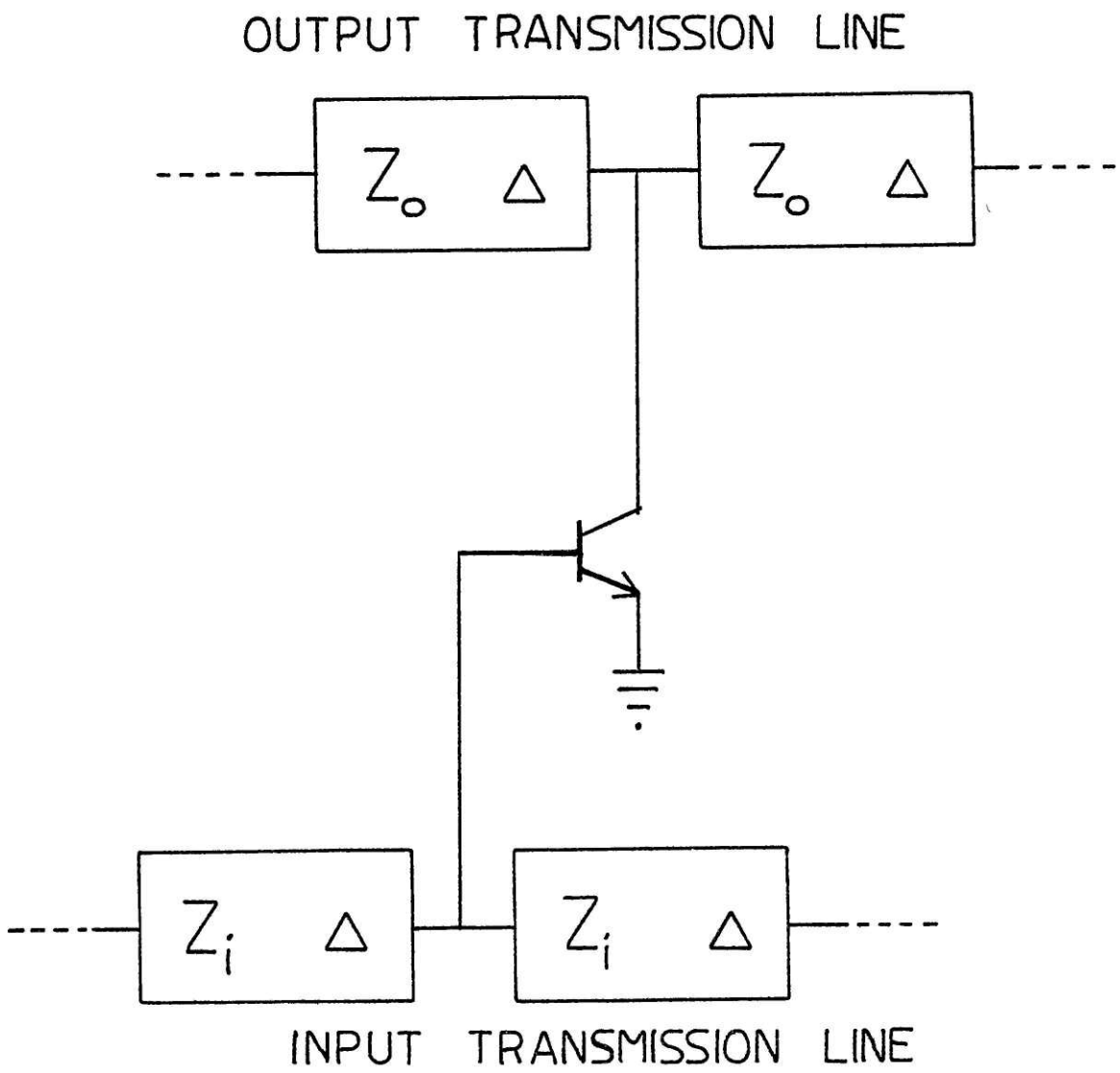

OUTPUT TRANSMISSION LINE
Z_o
Z_o
Z_i
Z_i
INPUT TRANSMISSION LINE

FIG. 2.5

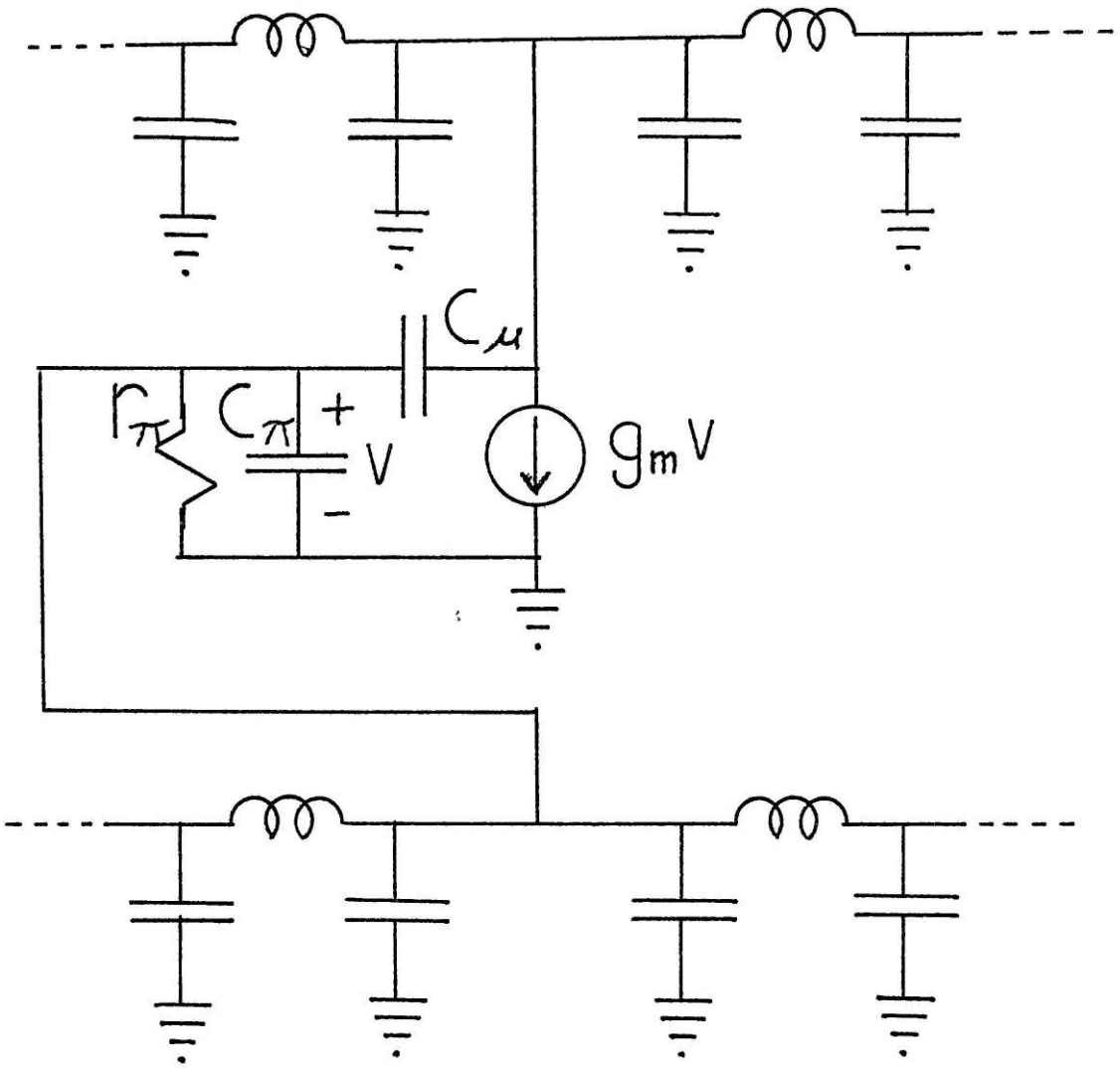


FIG. 2.6

be deferred to the next section.

The voltage gain of a single stage, G_o, can easily be verified to be,

$$G_o = \frac{g_m r_\pi Z_o'}{2Z_i' + 4r_\pi} \cong \frac{g_m Z_o'}{4}$$

where r_π is the incremental input resistance of the transistor, g_m is the incremental transconductance, Z_i' is the effective input transmission line characteristic impedance including the effects of C_π, and $Z_o' = Z_o$ is the output transmission line characteristic impedance. Therefore, the total power gain, G_p, is

$$\begin{aligned} G_p &= 2G_N{}^2 Z_i'/Z_o' \\ &= 2N^2 G_o{}^2 Z_i'/Z_o' \\ &\cong g_m{}^2 Z_o' Z_i' N^2/8 \end{aligned}$$

Again, the total power gain increases with the number of stages.

A more complicated distributed amplifier is shown in Fig. 2.7. This circuit makes use of three transmission lines, an input line, an output line, and an interstage line. The input and output lines function just as those described earlier, whereas the interstage line serves to isolate the output from the input, a useful function as will be shown in the next section.

The transistors connected to the input line are used as current amplifiers, while those connected to the output

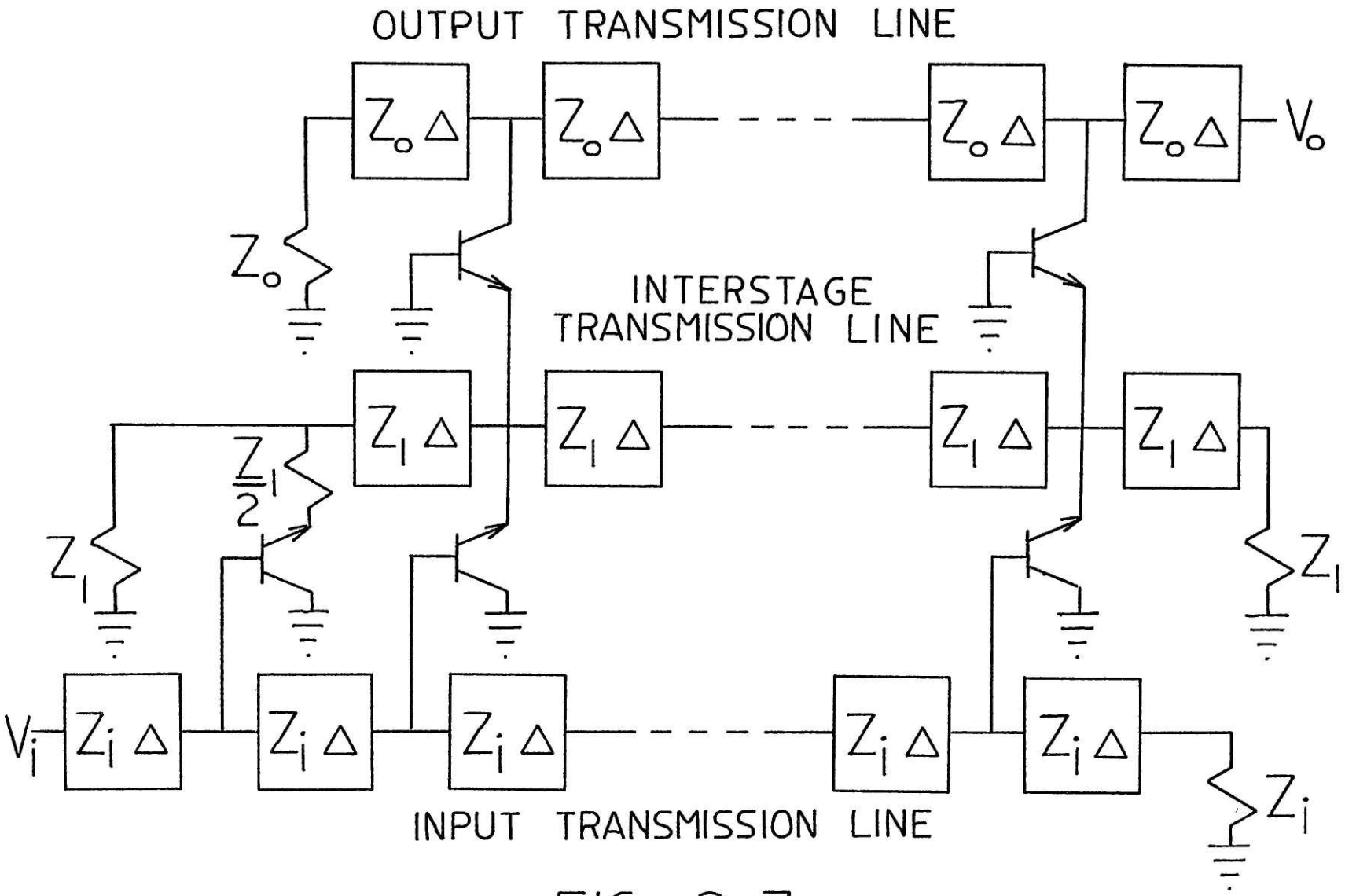

OUTPUT TRANSMISSION LINE
$Z_o\Delta$
$Z_o\Delta$
$Z_o\Delta$
$Z_o\Delta$
V_o
Z_o
INTERSTAGE
TRANSMISSION LINE
$Z_1\Delta$
$Z_1\Delta$
$Z_1\Delta$
$Z_1\Delta$
$\frac{Z_1}{2}$
Z_1
Z_1
V_i
$Z_i\Delta$
$Z_i\Delta$
$Z_i\Delta$
$Z_i\Delta$
$Z_i\Delta$
Z_i
INPUT TRANSMISSION LINE

FIG. 2.7

line are configured as voltage amplifiers. This circuit, then, provides both current gain and voltage gain.

The key to the operation of this circuit lies in the interstage transmission line. The first transistor fed by the input delay line is used to set up a voltage wave on the interstage line which is half the input voltage wave. Thus, when the signal propagating along the input line reaches the first amplifying stage, the incremental voltage from the base of the input transistor to the interstage line will be the same as the incremental voltage from the interstage line to the base of the output transistor. This produces the same current in each transistor and so there is no net current gained or lost by the interstage line. This means that the voltage wave present on it will continue propagating, unaltered, toward the second gain stage.

The current passed in this manner from the input transistor to the output transistor causes a voltage amplification in the common base output transistor which is fed, as before, onto the output delay line.

One final circuit variation will be mentioned here. If possible, it would be desirable to somehow use the entire signal generated by the output transistors as the output and not allow half of it to be dissipated in the reverse termination. One way in which to do this is to use a tapered output transmission line. Referring to Fig. 2.8, the output of the first gain stage is assumed to produce a current i_o. This is fed to an unterminated

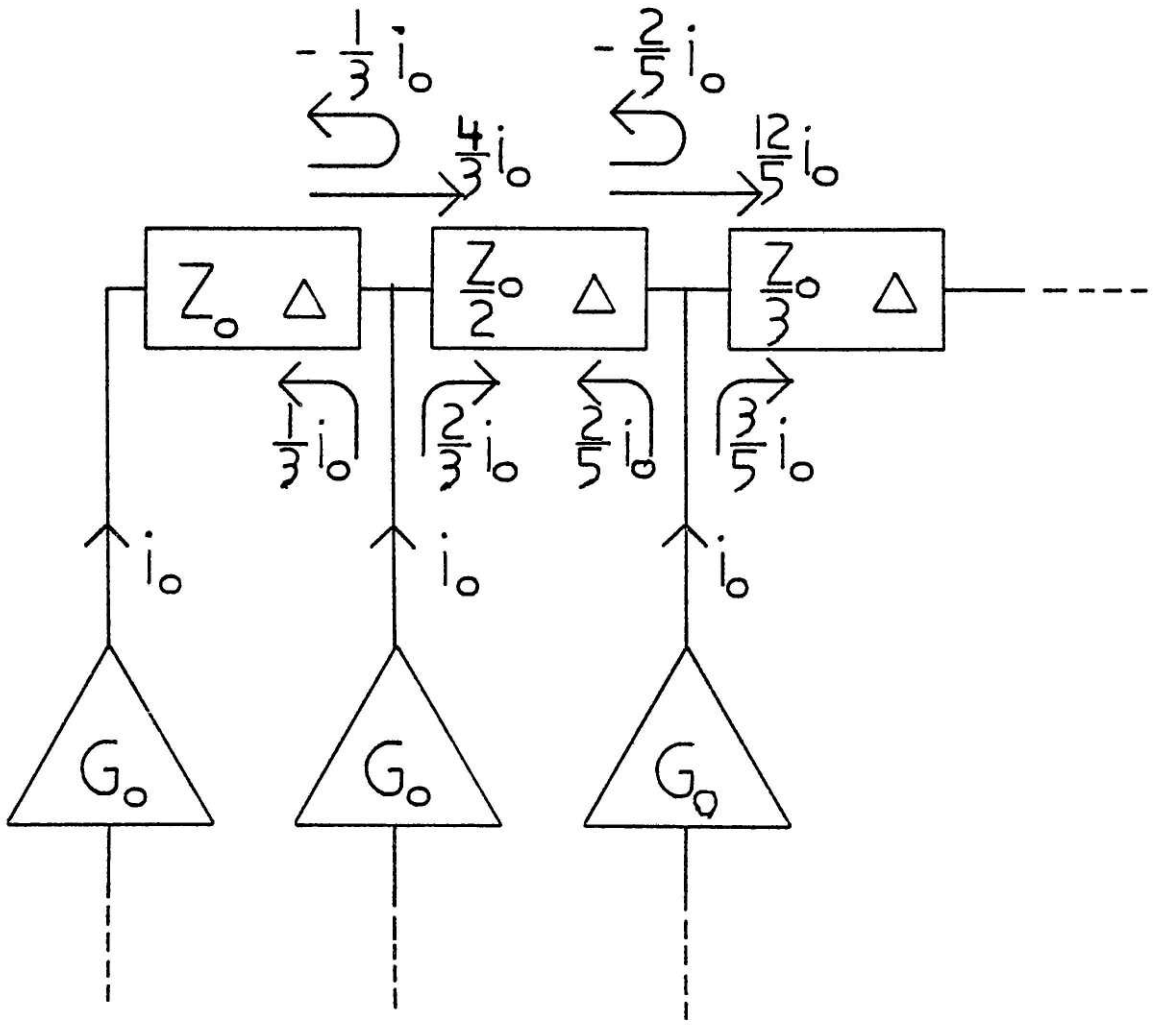

$-\frac{1}{3}i_o$
$-\frac{2}{5}i_o$
$\frac{4}{3}i_o$
$\frac{12}{5}i_o$
Z_o
$\frac{Z_o}{2}$
$\frac{Z_o}{3}$
$\frac{1}{3}i_o$
$\frac{2}{3}i_o$
$\frac{2}{5}i_o$
$\frac{3}{5}i_o$
i_o
i_o
i_o
G_o
G_o
G_o

FIG. 2.8

transmission line of characteristic impedance Z_o. At the output of the second gain stage, the characteristic impedance is changed to $Z_o/2$. This causes a reflection from this boundry such that a current wave of amplitude $-i_o/3$ is sent in the reverse direction and a current wave of amplitude $4i_o/3$ is sent in the forward direction. Because of the mismatch in characteristic impedances, the signal from the second gain stage will split unevenly. If the current from the second gain stage is the same as that from the first, then $i_o/3$ will flow in the reverse direction, exactly cancelling the reflected wave, and $2i_o/3$ will flow in the forward direction, making a total of $2i_o$ in this direction. Similarly, if at the output of the third gain stage the characteristic impedance is changed to 2/3 the previous value, or $Z_o/3$, a total of $3i_o$ will flow in the forward direction and no current will be sent in the reverse direction.

Clearly, if at the output of the n^{th} stage, the characteristic impedance of the output line changes from $Z_o/(n - 1)$ to Z_o/n, for all n, the total power developed at the output of the distributed amplifier will be twice that of the same configuration without the tapered line. At the same time, no power will be wasted in a reverse terminating impedance.

There are two major problems with distributed amplifier topologies in general, both of which have been ignored until now. The first has been alluded to and

involves coupling from the output transmission line to the input transmission line. Capacitive coupling, which can be found in most circuits from interlead capacitance, but which is especially troublesome in circuits such as the one employing the common emitter gain stage discussed earlier, is a form of positive feedback and leads to a prominent peak in the frequency response. For very high frequency amplifiers such instability increases rapidly with the number of stages and soon becomes intolerable.

One solution is to switch gain stages to devices which have less output-input coupling capacitance, such as a common base stage, or a design using MESFET (Ga-As) transistors. Another solution is to employ the circuit using the interstage line which has already been discussed. Signals which are coupled from the output to the interstage line are attenuated there so that they do not reach the input line, leading to a more stable frequency response.

The problem of input signal attenuation is also improved through the use of the interstage line. Since the two transistor design yields a higher effective impedance at high frequencies than does a single stage design, less of the input signal is lost at the input to each gain stage. This in turn, allows a higher number of stages to be used, which produces a higher overall gain.

TRANSMISSION LINES

Until recently, transmission lines were regarded as either too bulky to integrate or too unpredictable in terms of final characteristics to include "on chip".

Lumped element transmission lines were fully characterized and in use in many applications, but the difficulty in integrating a suitably sized inductor made integration a virtual impossibility. Microstrip transmission lines, on the other hand, in spite of widespread discrete use, had been fully characterized only for the extremes of a very narrow strip or a very wide strip.

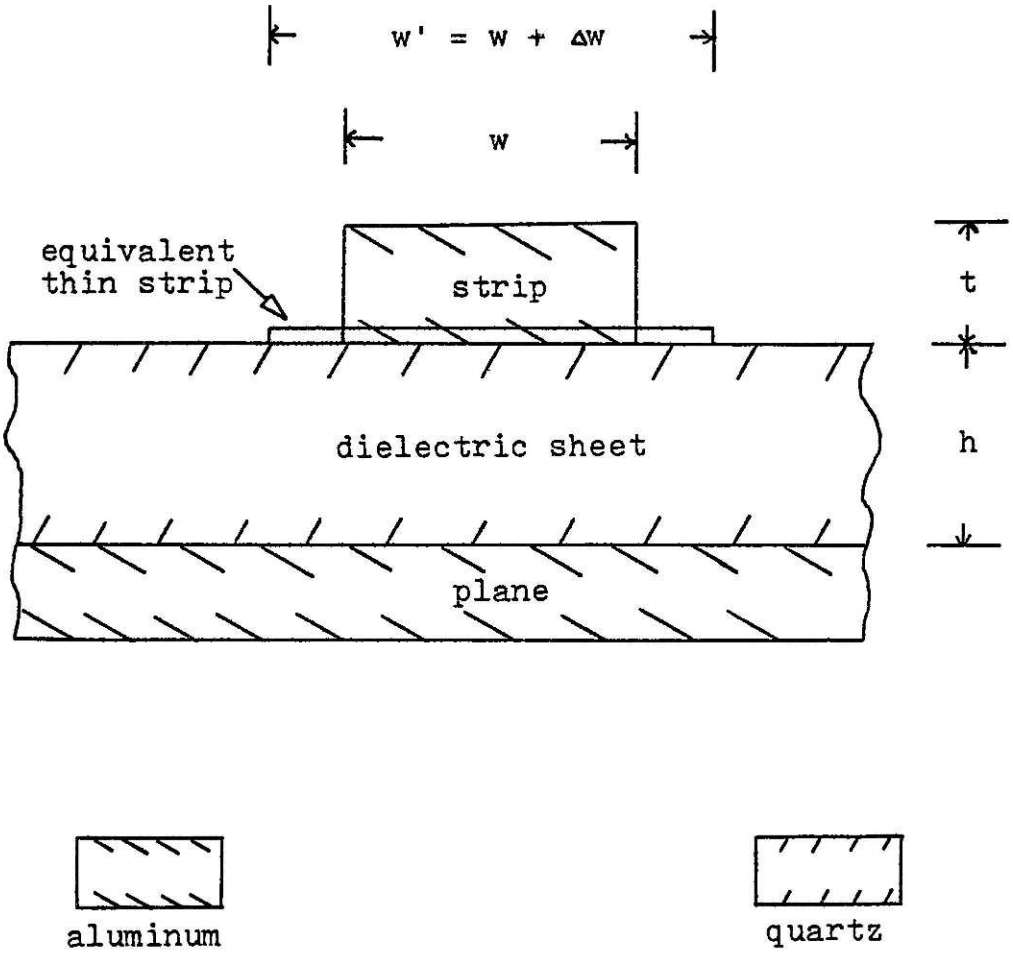
In March 1977, however, Harold A. Wheeler published in the IEEE Transactions on Microwave Theory and Techniques, a paper entitled "Transmission-Line Properties of a Strip on a Dielectric Sheet on a Plane". This paper combined the results of previous work on the subject of microstrip characterization and presented a group of formulas accurate to within two percent over the entire range of strip widths. Furthermore, it incorporated the effects of finite strip width on the calculation of the magnetic-loss power factor. The concentration here will be on the calculation of the required strip dimensions and the corresponding loss will be assumed to be within tolerable limits.

As pointed out in Wheeler's article, the difficulty in analyzing the "half-shielded" microstrip line comes in predicting quantitatively the effects of two different

dielectrics. Indeed, the interpolations between the wide strip and narrow strip cases are based mainly on empirical data. Nevertheless, the accuracy maintained by Wheeler is sufficient given the normal production tolerances for integrated circuits, so his formulas will be the ones used here.

The calculations derived by Wheeler are based on Fig. 3.1 and the following ideas. First, that the characteristic impedance of the microstrip is related to the characteristic impedance of a strip above a plane, with no intervening dielectric. This equivalent strip has a different but related width, and is easier to analyze, due to the uniformity in the dielectric. Second, that the effect of a finite strip thickness can be approximated by a change in the width of the equivalent stripline. Thus, in order to determine the characteristic impedance, the effective width of a suspended strip must be calculated from the true width, a width correction must be added to account for finite strip thickness, and finally, the characteristic impedance can be calculated using this adjusted width and previously derived formulas for the impedance of a thin strip with no dielectric.

If we label the characteristic impedance with dielectric R, the characteristic impedance without dielectric R1, the true width w, the width of an equivalent thin strip without dielectric w', the change in the true width due to thickness Δw, the change in equivalent width



MICROSTRIP CROSS-SECTION

FIG. 3.1

due to mixed dielectric $\Delta w'$, the height of the dielectric h, and the thickness of the stripline t, then the corresponding formulas are:

for R, $$R = \frac{42.4}{\sqrt{k+1}} \ln\left(1 + b\left[ab + \sqrt{a^2b^2 + \frac{k+1}{2k}\pi^2}\right]\right)$$

where $a = \frac{14k+8}{11k}$, and $b = \frac{4h}{w'}$;

for w'/h, $$\frac{w'}{h} = 8\,\frac{\sqrt{c\,\frac{7k+4}{11k} + \frac{k+1}{.81k}}}{c}$$

where $c = e^{\frac{R\sqrt{k+1}}{42.4}} - 1$;

for $\Delta w/t$, $$\frac{\Delta w}{t} = \frac{1}{\pi} \ln \frac{4e}{\sqrt{\left(\frac{t}{h}\right)^2 + \frac{t}{w\pi + 1.1\pi t}}}$$

and for $\Delta w'$, $$\Delta w' = \frac{(k+1)\Delta w}{2k}$$

where, in all cases, k is the dielectric constant of the dielectric sheet.

Using these formulas it is possible to program a digital computer to calculate one of the four design parameters (R, w, h, or t) given the other three. This was done using the APL facilities at IBM. In order to aid in trouble shooting the developed programs, each of the above equations (and two others found in Appendix A) were programmed individually. Next, a master program was written which would take the three known variables and compute the fourth. Its output is an ordered vector of all four values.

Finally, a user interface program was written which

takes a range and an increment size for each of three variables and repeatedly calls the master program for the fourth. The output of this function is a table of values suitable for direct output or for submission to a plotting routine.

The resulting APL programs and some representative results are contained in Appendix A. Each subroutine, in addition to being a functional block of the overall algorithm, can be called individually with the proper arguments for the cases when tabular output is not necessary or when only one point is to be calculated.

CIRCUIT LAYOUT AND SIMULATION

Recent implementations of distributed amplifiers have relied almost exclusively on MOS transistors fabricated on a gallium-arsenide substrate. MOS technology provides many advantages, among which are extremely low bias current, and simpler fabrication techniques. Ga-As semiconductors, on the other hand, yield devices with higher bandwidths. This is due to the higher minority carrier mobilities for such substances.

In contrast, bipolar silicon devices have their own advantages. Bipolar operation is generally faster than FET operation, while silicon fabrication boasts a wide variety of standardized processes which are easy to use and well characterized.

In order to demonstrate the feasibility of integrated distributed amplifiers, it is not necessary that the design be optimized for any particular application. For this reason, the practical aspects of process availability and fabrication time dictated that a standard analog bipolar technique, currently in use at IBM, be used for the devices.

This choice offered a further advantage. Design and layout time could be shortened through the use of a standard mix of resistors and active elements, over which the customized metalization would be placed. The use of such master wafer patterns is fairly common in industry

and fabrication processes are undoubtedly similar, but specific information about them remain company secrets. For this reason, only the characteristics of the final devices will be given here.

In order to assure matched devices and to allow comparisons between differing circuit topologies, the same size transistor was used throughout. Minimum specifications for this transistor include, I_{Cmax} = 4 ma, h_{FE} = 20, and f_T = 400 MHz.

Having selected the circuit elements, the next step in the development process was to decide which circuit topologies to use. In specific, the details of the generalized gain block of Fig. 2.1 had to be determined along with the number of stages to be used. To do this, digital simulation of several possible configurations was undertaken. Fairly detailed models for the devices chosen as circuit elements had already been developed for use with IBM's Advanced STatistical Applications Program (ASTAP), so this circuit analysis program was chosen.

The model used by ASTAP is a modified Ebers-Moll model and is depicted by the schematic of Fig. 4.1. Note that a fourth terminal must be provided to model the interactions with the substrate.

Although ASTAP has provisions for statistical variations in device parameters, this feature was not used, mostly because of the simplicity of the circuit and

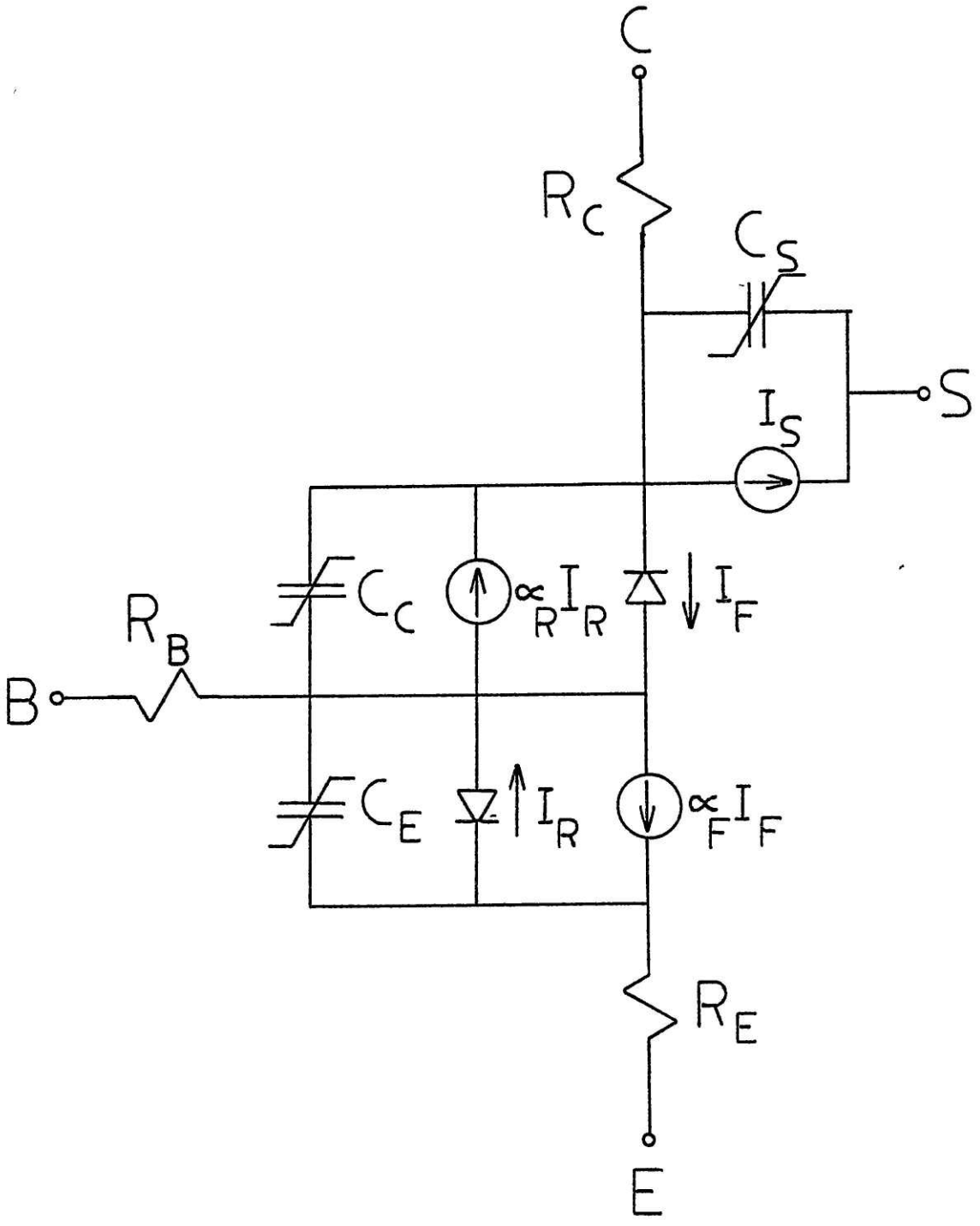


FIG. 4.1

the interest in faster turn around times. Similarly, it was felt that transient response (i.e. step response) analysis would serve to point out issues such as delay, and stability more clearly than frequency domain analysis, therefore transient analysis was the only mode of analysis used.

A comprehensive list of the different topologies, operating points, and small signal inputs simulated is left for Appendix B in the interest of brevity, but a typical run will be presented here as an example of the results obtained.

The circuit to be analyzed is presented schematically in Fig. 4.2. It is a ten stage distributed amplifier with common base stages and equal input and output transmission line impedances. The input voltage before the step input is -1.45 volts. This establishes a transistor collector bias current of about 45 μa.

The results of the ASTAP transient analysis are tabulated in Fig. 4.3 and plotted versus time in Fig. 4.4. From this graph it is possible to identify several important features. First of all, though it may be possible to measure the delay due to the transmission lines, it is clearly negligible compared to that introduced by the input capacitance of the first transistor. In other words, the terminal characteristics of this amplifier will not include a pure delay. Though this is not important for proper circuit operation, it would be one indication of

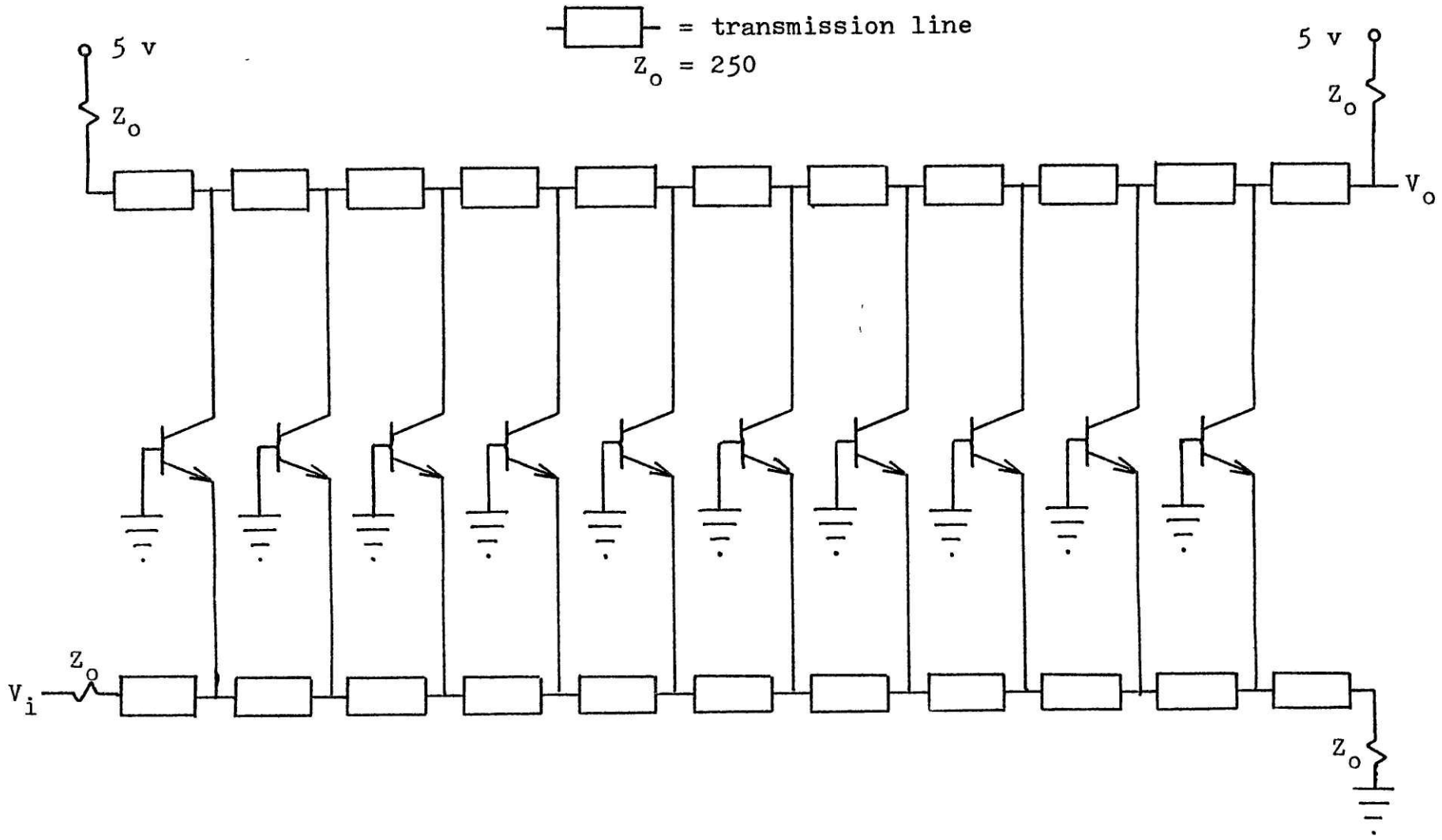


FIG. 4.2

COMPUTER SIMULATED STEP RESPONSE

TEN STAGE COMMON BASE AMPLIFIER

(input amplitude = .1 v)

Time (nsec)	Output Voltage (volts)
0.0	4.944
0.025	4.944
0.05	4.934
0.075	4.934
0.1	4.933
0.125	4.931
0.15	4.929
0.175	4.925
0.2	4.921
0.25	4.911
0.3	4.900
0.35	4.890
0.4	4.880
0.45	4.871
0.5	4.863
0.55	4.856
0.6	4.849
0.7	4.838
0.8	4.829
0.9	4.822
1.0	4.817
1.2	4.811
1.4	4.807

FIG. 4.3

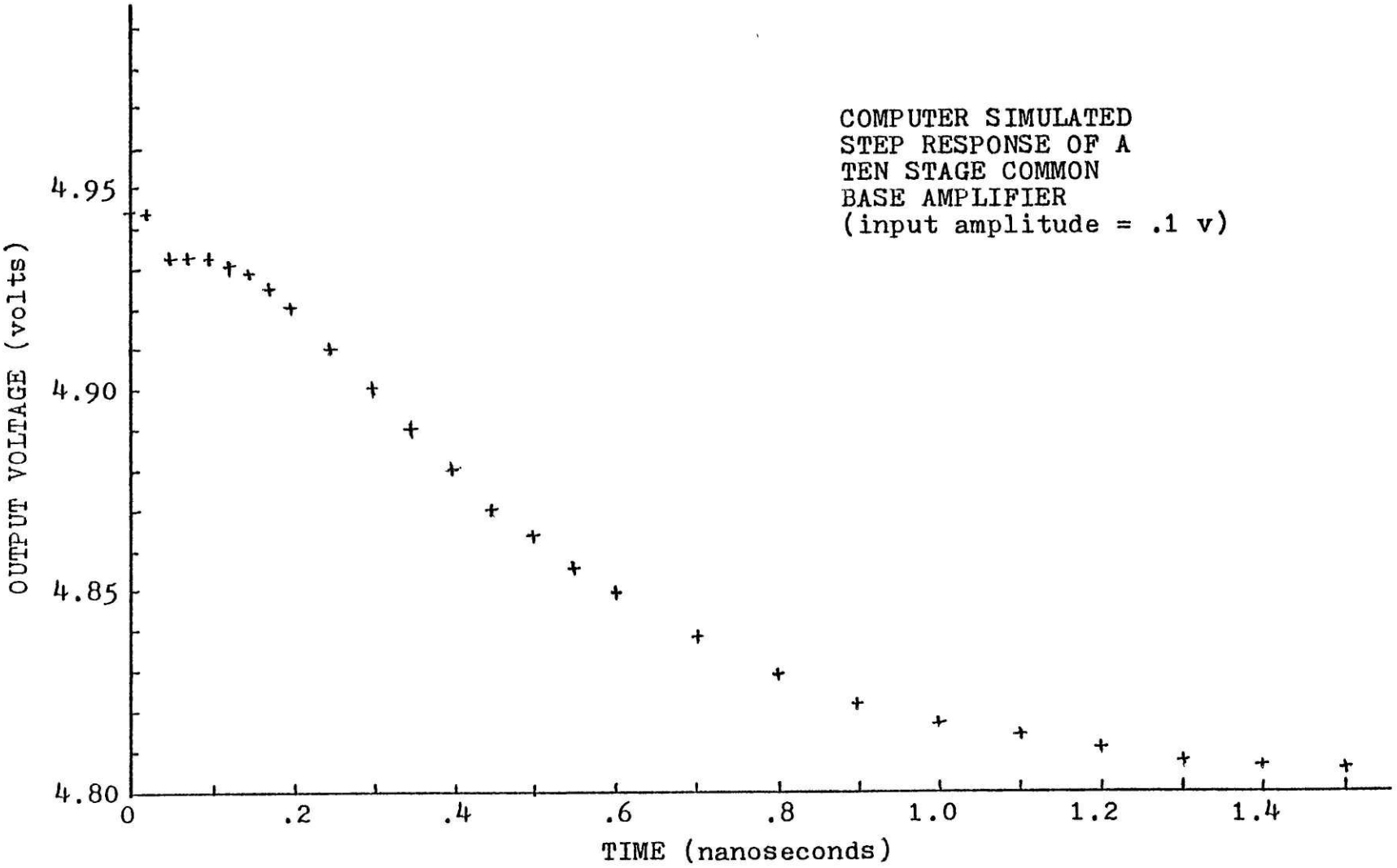

COMPUTER SIMULATED
STEP RESPONSE OF A
TEN STAGE COMMON
BASE AMPLIFIER
(input amplitude = .1 v)
OUTPUT VOLTAGE (volts)
4.95
4.90
4.85
4.80
0
.2
.4
.6
.8
1.0
1.2
1.4
TIME (nanoseconds)

FIG. 4.4

distributed operation if it were present.

Secondly, the gain of the distributed amplifier is much less than the cookbook common base gain, Z_o/Z_i, due to terms in the gain expression which are usually negligible. Further, the fact that the DC gain is greater than the expected single stage gain does not suggest distributed operation either since paralleling transistors would yield the same result.

Finally, note that the response to a step input appears first order, except for an initial delay. This suggests that the circuit has one dominant pole, whose location can be estimated by the initial slope of the step response.

These points are applicable to all the circuits simulated and are therefore the basis for comparisons between them. From the graph of Fig. 4.4 it is possible to determine both the gain and the initial slope of the response, m_o. From these, the gain-bandwidth product can be calculated as,

$$GxBW = G_p m_o/(v_{final} - v_{initial})$$

This number is an excellent indicator of distributed operation, since it should increase with the number of stages for a distributed amplifier, but remain the same for a parallel connection of stages. For the graph of Fig. 4.4,

$$G_p = .2 \quad ,$$

$$V_{final} - V_{initial} = -.14 \text{ volts} \quad ,$$

and $$m_o = -2.2 \times 10^8 \text{ volts/sec} \quad .$$

From these measurements, the gain-bandwidth product is,

$$GxBW = 4.9 \times 10^8 \text{ Hz} \quad .$$

This is an improvement of about a factor of one hundred over the results obtained for a similarly connected single transistor conventional amplifier. (See Appendix B.) Similar results can be obtained for amplifiers with different numbers of stages. These results have been summarized in the graph of Fig. 4.5.

Based on these figures and the available literature, several amplifier topologies were selected for fabrication. It was felt that by using a large number of different circuits, any problems encountered could be more effectively analyzed.

As a result of the layout system used at IBM, it was possible to have four different chips processed on the same wafer. This added to the diversity that could be achieved, and full advantage was taken of it. Although test devices had to be manufactured for process monitoring purposes, these devices could not be depended upon, since they nearly always were destroyed by wafer dicing. Thus it was decided that one of the four chips would need to be dedicated solely to test devices. On this chip were placed individual test transistors, single stage amplifiers, and sample lengths of microstrip. In addition to providing

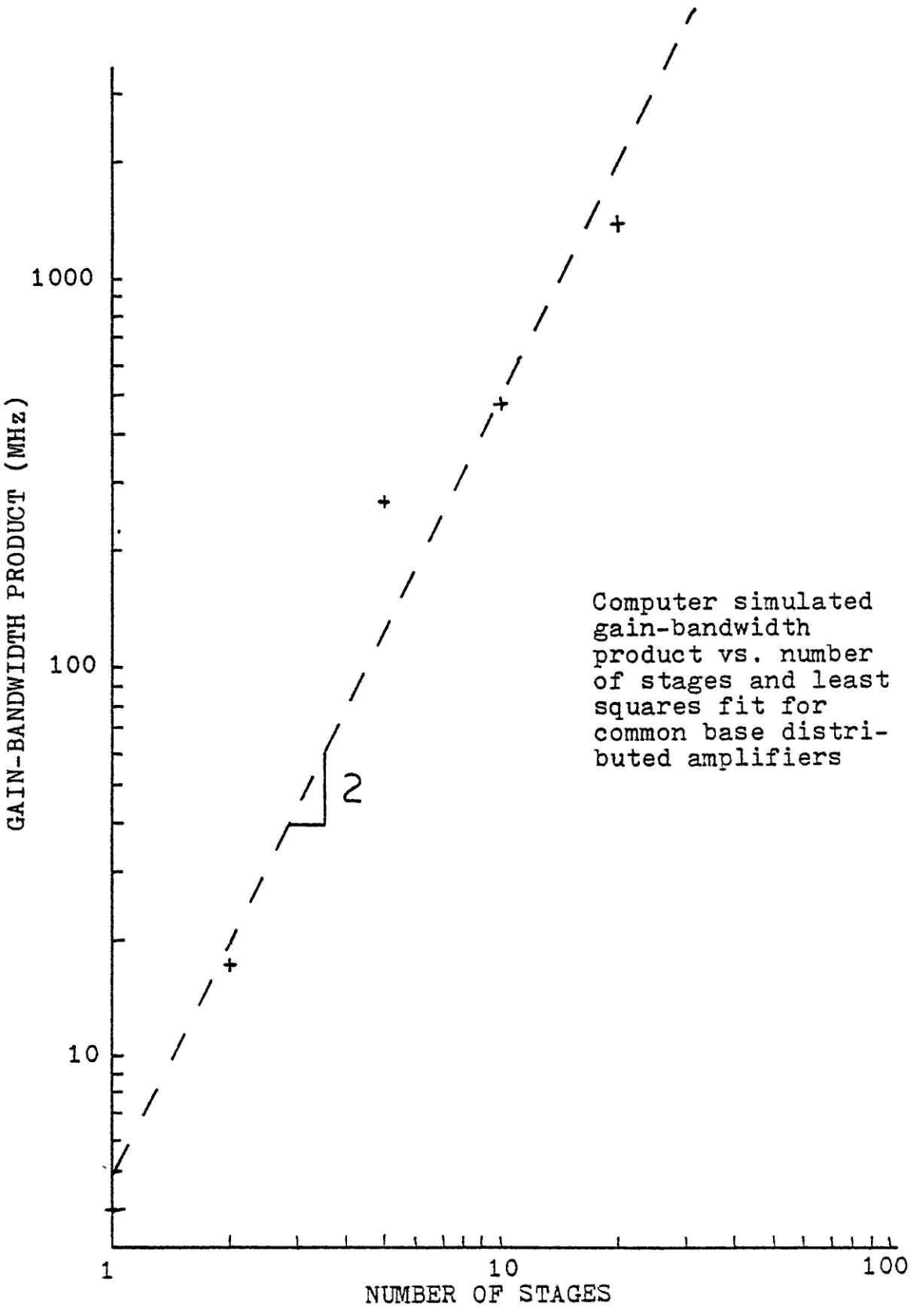

GAIN-BANDWIDTH PRODUCT (MHz)
1000
100
10
2
1
10
100
NUMBER OF STAGES
Computer simulated gain-bandwidth product vs. number of stages and least squares fit for common base distributed amplifiers

FIG. 4.5

individual circuit elements for error location, these components would later be used as standards against which to measure the performance of the main amplifiers.

The remaining three chips were large enough to accomodate a few large circuits or several smaller circuits. For simplicity in later identification, it was decided that each chip should be dedicated to a specific gain stage. The two most logical choices, based on the results of the computer simulation, were the common base stage for high bandwidth, and the common emitter stage for high gain. Both were simple enough to present few anticipated problems and both had been simulated enough to show a substantial expected increase in gain-bandwidth product. Also, the similarity of the gain stages topographically made the layout of the circuits similar.

Computer simulation had indicated that the greatest gain-bandwidth product was attained by the largest number of stages. For this reason, it was decided that a twenty stage design should be attempted. As this required a dimension longer than the chip width, the circuit outline resembled that of a horseshoe, and used up a major portion of the chip periphery. The remainder of the chip was found to accomodate two eight stage designs. Thus for the common base and the common emitter designs, there were a total of four different amplifiers integrated: a twenty stage design, two similar eight stage designs,

and a single stage design on the test chip.

Optimistically, the final chip was used for an advanced design. Several possibilities were considered, but it was finally decided that the two transistor gain stage had the highest probability of succeeding. Because of uncertainties in the input and output capacitances and because of difficulties in obtaining a wide range of transmission line characteristic impedances, circuits such as the tapered impedance output line amplifier discussed previously were not felt to be feasible. Area limitations allowed only two similar twelve stage designs to be implemented using the two transistor gain stage. Nevertheless, four different circuits relating to this design were constructed: the two main amplifiers, a single stage amplifier, and a single amplifier stage. These last two were on the test chip.

TESTING AND RESULTS

As is the case with most developmental integrated circuits, the processing needed for this project was more efficiently provided by the small volume facilities associated with the IBM, Endicott location. These were readily made available to me, although for safety considerations, the personnel affiliated with the wafer processing department did the actual production work.

In a preliminary first pass test, the devices on the test chip yielded meaningful results, indicating that the processing had been accomplished without flaw, but it was shortly discovered that, in spite of the elaborate topology testing programs used to check the actual chip layout against the circuit schematic, the ground plane (located on the first level of metal) on each of the common base and common emitter chips was not electrically connected to the ground pad to be used for wire bonding.

This problem was overcome, however, by selectively etching away the pad and intervening quartz. This left the ground plane exposed as the top level of metal and wire bonding could then proceed. The remainder of the circuit was protected during this process by an inert wax. Hydrochloric acid was used to remove the ground pad, while concentrated hydroflouric acid was used to etch the quartz. This procedure was found to yield the best results.

Unfortunately, when dealing with chemicals of such

strength, it is very difficult to completely protect the rest of the circuit. In this instance, the wax performed quite nicely, but the proximity of some of the circuit components to the ground pad and the difficulty in applying the wax by hand combined to render the twenty stage circuits inoperable on those chips so processed. It seems that practice and patience would eventually prevail, but because the smaller circuits remained functional, it was decided to characterize them and return to the larger circuits only if necessary.

The use of a wafer/chip prober was adequate enough for initial test and evaluation, but complete device characterization required the chip to be mounted and contacted in a more permanent manner. Several mounting schemes were considered, but it was decided that the advantages of reliability, ease of use, and device protection offered by a ceramic substrate far outweighed the disadvantages of cost, production delay, and inflexibility.

The substrate was approximately one inch square and connections to the chip were made via 50 ohm microstrip transmission lines and a ground pad which connected to the ground plane on the reverse side. The chip under test was attached to the substrate with silver paint. Similarly, the substrate was attached to the mounting block with silver paint and connections to the substrate were made with removable SMA to microstrip transitions

mounted to the mounting block. Gold wire bonding was used to connect the substrate microstrip to the chip pads.

The first step in the testing procedure was to verify the results obtained with the wafer probe. This portion of the test was mainly concerned with circuit continuity and low frequency characteristics; parameters necessary for further test, such as beta, collector-emitter saturation voltage, and collector-emitter sustaining voltage were determined here. Typical values were, $\beta = 36$, $V_{CE(sat)} = .2$ volts, and $V_{CE(sus)} = 27$ volts.

The next step in the testing procedure was to determine the frequency response of the circuits and compare them with similar measurements made on the test devices. Preliminary estimates were obtained from spectrum analysis using Tektronix plug-in equipment. Although this was adequate to give a general picture of the results, a more accurate final measurement was deemed desirable.

Toward this end, the frequency measurements were duplicated on a Hewlett-Packard 8505A Spectrum Analyzer. This system had the added advantage of being set up to perform bulk measurements under the control of a Tektronix 4051 mini-computer. This system is far from being standard, but the functions performed by it are straightforward. The 4051 controls a precision waveform generator which in turn drives the 8505A. The measurements taken by the 8505A are then digitized and stored by the 4051. Calibration is also controlled by the 4051, and the results

are available in a variety of different formats. Commonly, s-parameters are used to describe circuits in this frequency region, so this is the form that will be used here.

In order to get a detailed representation of the circuits tested a large number of measurements were made. In specific, circuit properties were determined both as a function of frequency and as a function of operating point. Because of the large number of measurements involved and in light of the time required to complete each set of measurements, only four circuits were fully tested. These were the single stage common base and common emitter designs, and the eight stage common base and common emitter designs.

Nevertheless, the number of results obtained is still far too large to be presented here, so this will be left for the appendices. Instead, one representative sample from each of the circuits analyzed will be presented and the general results shown in Appendix C will be stated.

In order to provide an extra degree of flexibility, the termination resistors for the circuit transmission lines had been included as "options" for the twenty stage amplifiers. Space limitations prevented their inclusion in the eight stage versions. In addition, it was found that to provide an appreciable bias voltage to the transistors, an excessive amount of current had to be passed through such terminations. Off chip resistors or

coupling capacitors seemed reasonable but difficult solutions until it was noted that because of the chip dimensions, the minimum expected signal wavelength was still much larger than the maximum circuit dimension.

This meant that the standing waves which would be set up if the termination connections were left open would not interfere with the proper operation of the circuit. The lack of a termination impedance on the output line doubles the load seen by the gain stage outputs. This, in turn, doubles the voltage found at the load resistor. Therefore, the elimination of the termination impedance causes a factor of four increase in the overall power gain.

Similarly, removing the input termination impedance causes an identical power gain increase. To see this, note that as long as the line characteristic impedance is much smaller than the input impedance of the parallel gain stages, the lack of a termination resistor is responsible for a factor of two increase in the voltage seen at the gain stage inputs. This corresponds to a factor of four increase in the measured output power.

This simplification made wire bonding and circuit test easier. For example, the bias currents (assuming matched transistors) were now directly measurable, instead of having to be estimated from the voltage at the amplifier input. For these reasons, all measurements were carried out without termination resistors.

The results of the spectrum analysis for the single stage common emitter amplifier indicate that there is a maximum in the gain-bandwidth product for an emitter current of about 200 μamperes. For this reason, this set of measurements has been chosen for presentation here. The measured s-parameters are tabulated in Fig. 5.1. The important parameter for this discussion is s_{21}, which is plotted in Fig. 5.2. From these figures the low frequency gain is seen to be about 13 dB ($P_{out}/P_{in} = 20$), and the bandwidth is close to 65 MHz. This makes the gain-bandwidth product 1.3 GHz.

Analogous results are obtained for the eight stage amplifier. Operating at an output bias current of 2 milliamperes, the results of the spectrum analysis are shown graphically and in tabular form in Fig. 5.3 and 5.4. From these we can obtain,

$$G_p = 83 \text{ (19 dB)}$$

and

$$BW = 78 \text{ MHz} \quad .$$

Note that it becomes difficult to estimate the bandwidth because of the ripple in the frequency response, which is substantial in this case. This phenomenon has not been fully explained, but it is similar to the stability problems mentioned in a previous section. Further testing with a higher number of stages would help resolve this question. The gain-bandwidth product for the values above is,

$$GxBW = 6.5 \text{ GHz} \quad .$$

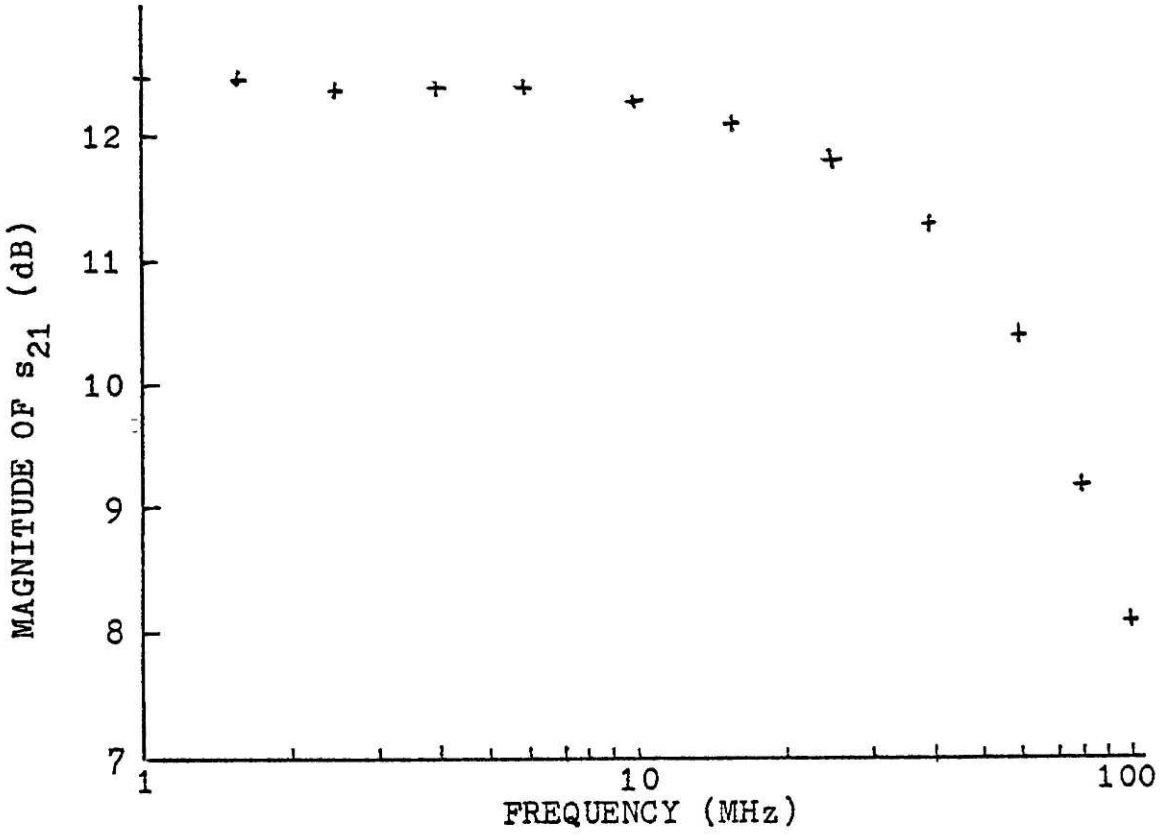
MEASURED S-PARAMETERS

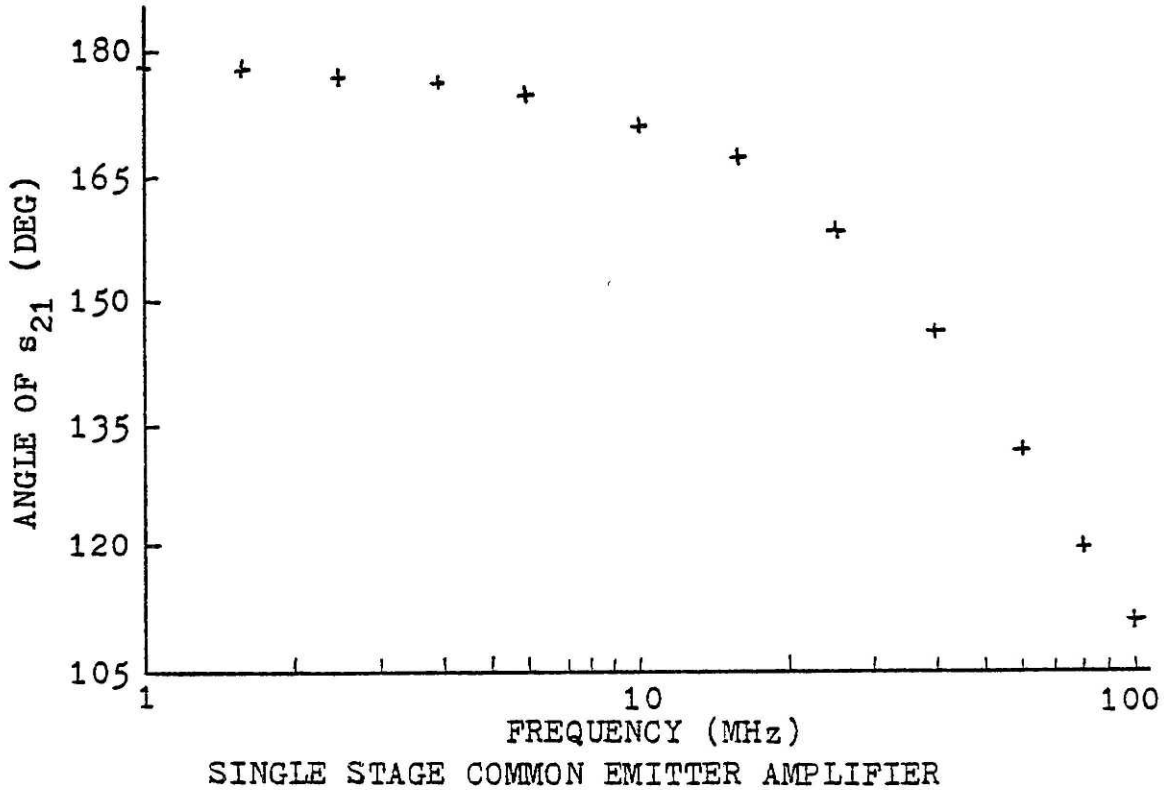
SINGLE STAGE COMMON EMITTER AMPLIFIER

FREQUENCY MHz	S_{11} MAGNITUDE dB	S_{11} ANGLE DEG	S_{12} MAGNITUDE dB	S_{12} ANGLE DEG
1	-1.52	-0.3	-76.2	56.3
1.5	-1.52	-0.5	-81.1	20.2
2.5	-1.52	-0.9	-76.8	36.8
4	-1.52	-1.5	-75.8	52.9
6	-1.53	-2.3	-73.0	58.9
10	-1.54	-3.7	-68.5	69.3
15	-1.57	-5.5	-66.1	70.2
25	-1.69	-8.9	-62.4	70.8
40	-1.98	-13.5	-58.6	66.8
60	-2.43	-18.6	-55.8	60.8
100	-3.26	-26.1	-53.0	54.5

FREQUENCY MHz	S_{21} MAGNITUDE dB	S_{21} ANGLE DEG	S_{22} MAGNITUDE dB	S_{22} ANGLE DEG
1	12.5	178.1	.010	0.1
1.5	12.5	177.8	.020	0.0
2.5	12.4	176.9	.019	-0.2
4	12.4	176.4	.024	-0.5
6	12.4	174.9	.025	-0.8
10	12.3	171.3	.018	-1.5
15	12.1	167.0	.001	-2.2
25	11.8	158.3	-.001	-3.7
40	11.3	146.3	-.018	-5.9
60	10.4	132.2	-.070	-8.7
100	8.1	111.0	-.121	-14.0

FIG. 5.1





SINGLE STAGE COMMON EMITTER AMPLIFIER

FIG. 5.2

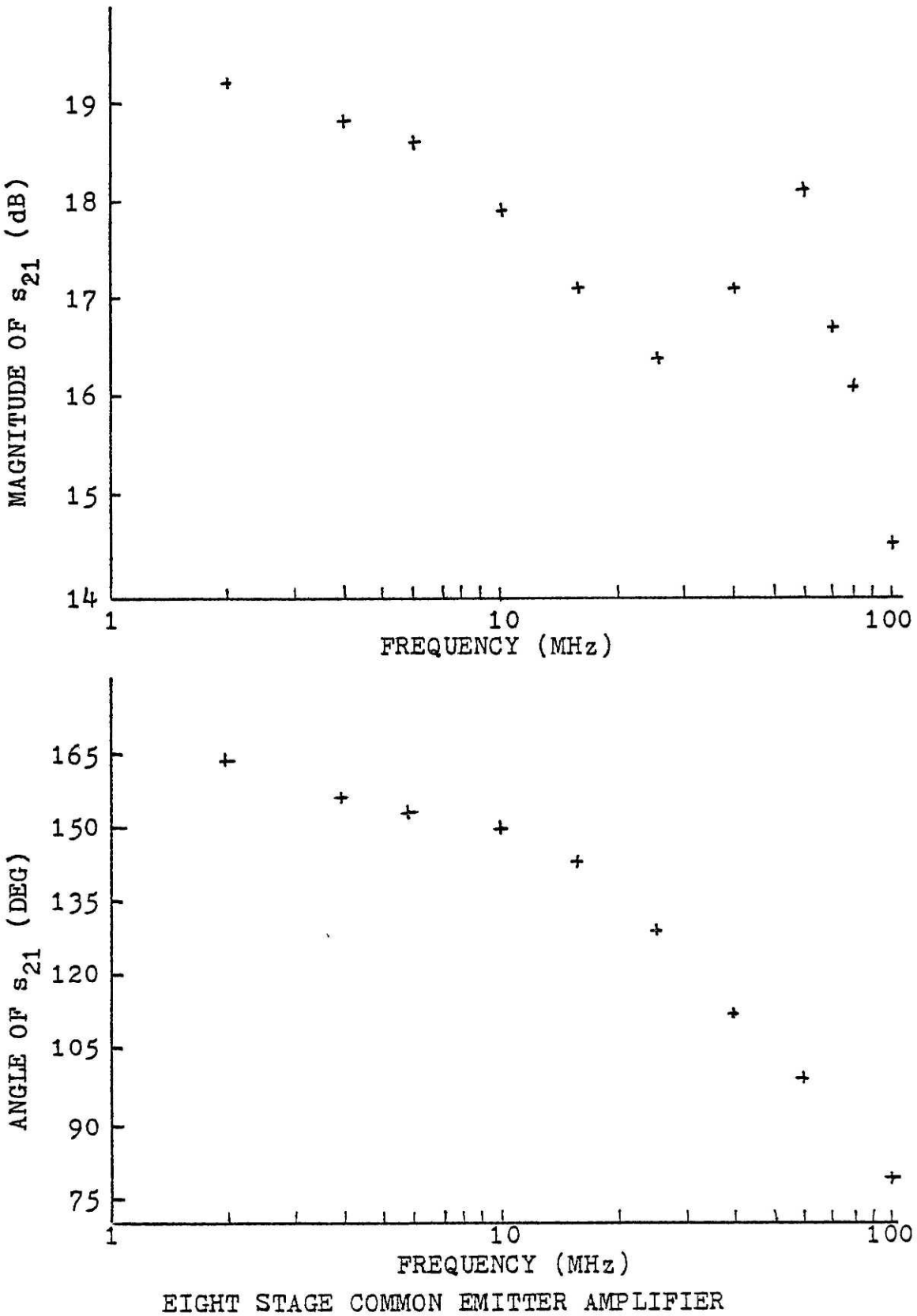
MEASURED S-PARAMETERS

EIGHT STAGE COMMON EMITTER AMPLIFIER

FREQUENCY MHz	S_{11} MAGNITUDE dB	S_{11} ANGLE DEG	S_{12} MAGNITUDE dB	S_{12} ANGLE DEG
2	-25.2	-34.1	-57.5	25.5
4	-22.9	-56.5	-55.4	40.4
6	-20.8	-72.0	-53.1	48.9
10	-17.4	-91.6	-49.5	54.0
15	-14.9	-105.0	-47.0	53.3
25	-11.8	-125.0	-43.6	48.3
40	-9.8	-142.8	-41.4	41.6
60	-8.7	-155.0	-40.1	37.4
100	-7.8	-171.0	-38.6	36.4

FREQUENCY MHz	S_{12} MAGNITUDE dB	S_{12} ANGLE DEG	S_{22} MAGNITUDE dB	S_{22} ANGLE DEG
2	19.2	164.5	-0.82	-1.1
4	18.8	156.9	-0.79	-3.1
6	18.6	154.3	-0.83	-5.2
10	17.9	150.6	-1.04	-9.2
15	17.1	143.9	-1.36	-12.9
25	16.4	130.4	-2.15	-19.2
40	17.1	113.1	-3.16	-24.4
60	18.1	99.0	-4.01	-27.9
100	14.5	79.0	-4.83	-33.8

FIG. 5.3



EIGHT STAGE COMMON EMITTER AMPLIFIER

FIG. 5.4

Even with the lower value of bandwidth (30 MHz), the gain-bandwidth product can be seen to have improved significantly (2.5 GHz vs. 1.3 GHz).

The results for the common base configuration are not troubled by the high frequency ripple as would be expected if that ripple were indeed caused by coupling between the output and input transmission lines. The measured parameters, using the same system as in the common emitter case, for the single stage common base amplifier are listed numerically in Fig. 5.5, while the magnitude and phase of s_{21} are graphed in Fig. 5.6. From these figures the gain and bandwidth can be calculated as,

$$G_p = 1.7 \text{ (2.4 dB)}$$

and $$BW = 350 \text{ MHz} \quad .$$

Thus, $$GxBW = 600 \text{ MHz} \quad .$$

Note that near the top end of the frequency range, the gain of a single stage is less than unity.

Focusing our attention on Figs. 5.7 and 5.8, which contain the measured results for the eight stage common base amplifier, we see that

$$G_p = 3.3 \text{ (5.2 dB)}$$

and $$BW = 625 \text{ MHz}$$

and that, as predicted, the gain-bandwidth product has increased to

$$GxBW = 2.1 \text{ GHz} \quad .$$

Remembering that each individual stage is operating at

MEASURED S-PARAMETERS

SINGLE STAGE COMMON BASE AMPLIFIER

	S_{11}		S_{12}	
FREQUENCY MHz	MAGNITUDE dB	ANGLE DEG	MAGNITUDE dB	ANGLE DEG
25	-8.67	161.2	-57.3	74.6
40	-8.43	150.9	-53.7	73.1
60	-8.17	137.4	-50.0	70.6
100	-7.62	112.5	-45.8	63.0
150	-6.97	86.5	-43.0	53.7
250	-5.86	47.1	-40.0	38.6
400	-5.01	5.7	-38.0	21.9
500	-4.80	-16.5	-37.3	13.6

	S_{21}		S_{22}	
FREQUENCY MHz	MAGNITUDE dB	ANGLE DEG	MAGNITUDE dB	ANGLE DEG
25	2.37	-8.6	.038	-3.4
40	2.35	-13.7	.026	-5.5
60	2.25	-20.4	.014	-9.6
100	1.92	-33.5	.006	-13.7
150	1.30	-48.6	-.007	-20.4
250	-0.03	-75.4	-.020	-33.4
400	-2.03	-109.1	-.117	-53.6
500	-3.35	-129.2	-.151	-67.2

FIG. 5.5

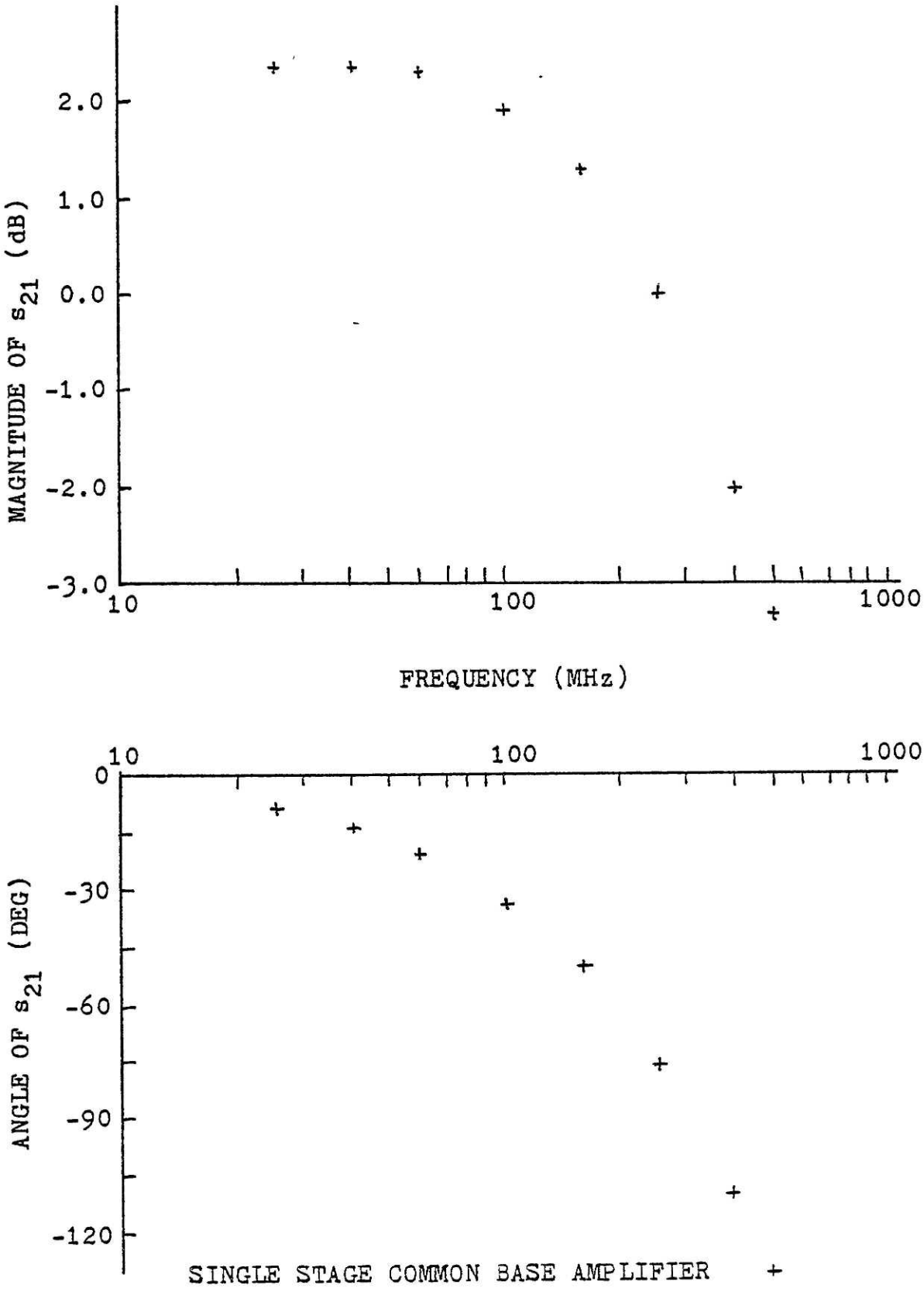

MAGNITUDE OF s_{21} (dB)
2.0
1.0
0.0
-1.0
-2.0
-3.0
10
100
1000
FREQUENCY (MHz)
ANGLE OF s_{21} (DEG)
0
-30
-60
-90
-120
SINGLE STAGE COMMON BASE AMPLIFIER

FIG. 5.6

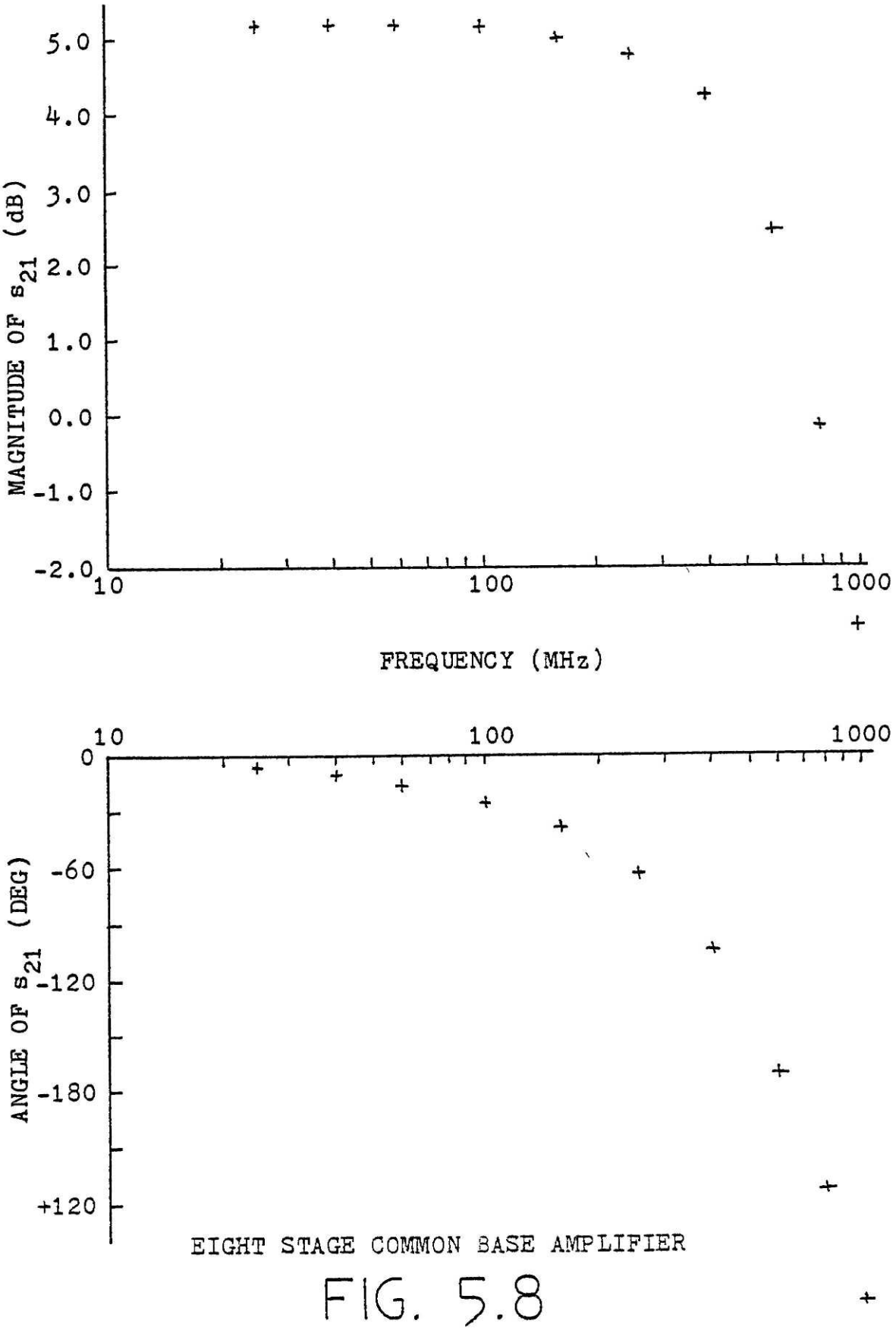
MEASURED S-PARAMETERS

EIGHT STAGE COMMON BASE AMPLIFIER

	S_{11}		S_{12}	
FREQUENCY MHz	MAGNITUDE dB	ANGLE DEG	MAGNITUDE dB	ANGLE DEG
25	-1.12	174.5	-51.1	84.7
40	-1.13	171.3	-47.3	87.2
60	-1.12	167.0	-43.3	89.7
100	-1.15	158.5	-38.3	92.2
150	-1.19	148.2	-34.0	92.8
250	-1.26	127.1	-27.8	87.6
400	-1.40	95.3	-21.4	71.9
600	-2.13	54.4	-16.5	32.3
1000	-4.86	-11.6	-12.3	-28.0

	S_{21}		S_{22}	
FREQUENCY MHz	MAGNITUDE dB	ANGLE DEG	MAGNITUDE dB	ANGLE DEG
25	5.20	-6.2	.011	-5.6
40	5.19	-9.9	.003	-9.1
60	5.18	-14.9	-.011	-13.8
100	5.15	-25.2	-.043	-22.7
150	5.03	-38.1	-.082	-33.8
250	4.80	-63.5	-.185	-56.4
400	4.28	-103.5	-.507	-93.6
600	2.52	-170.9	-1.701	-147.4
1000	-2.78	68.8	-5.352	104.3

FIG. 5.7



EIGHT STAGE COMMON BASE AMPLIFIER

FIG. 5.8

the same collector current as in the single stage measurements, and that in the upper frequency range, therefore, the gain of each stage is less than unity, the gain of the overall amplifier is greater than unity.

These general results hold fairly uniformly for all the samples tested, i.e. the gain-bandwidth product does increase with the number of stages, indicating that the circuits are functioning in a distributed mode. Some surprising results are as follows.

First, it would be expected that the bandwidth of the complete amplifier should decrease with collector current since the input capacitance increases with increasing collector bias current. This does not appear to be the case, at least not with the common base configuration. This may be true of the common emitter amplifier, but the presence of the peaking in the frequency response makes it difficult to determine.

Next, it can be seen from the data in the appendices that the gain of the common emitter amplifier is maximized for a particular value of collector bias current. This is not necessarily a general result, however, as it can be accounted for by the colloctor current dependence of β, the current gain of the transistor, which for this batch displayed a maximum at the same value of current per stage. Since emitter-collector current gain, α, displays a similar peak, it would stand to reason that such might be observed in the frequency response of the

common base amplifier. This does not occur, however, indicating that some other factor (such as the dependence of g_m or f_T on collector current) is the overriding concern in the determination of the gain-bandwidth product.

One last item of interest involves the predicted results presented in an earlier section. For comparison, the test results for the eight stage common base amplifier operated at an output bias current of 2 milliamperes will be used. The results of this test are shown in Figs. 5.9 and 5.10. As before, the gain and bandwidth are calculated from these to be,

$$G_p = 2.1 \ (3.2 \text{ dB})$$

and

$$BW = 560 \text{ MHz} \quad ,$$

yielding a gain-bandwidth product of

$$GxBW = 1.2 \text{ GHz} \quad .$$

In order to permit a meaningful comparison, the previous results must be adjusted to account for differences between the two circuits. If the results for a ten stage amplifier operated at a similar bias current are chosen for comparison, the following changes must be made. Two factors of four account for the lack of termination impedances. The voltage gain differs by a factor of .8 due to the decrease in the number of stages. The power gain is scaled by a factor of .2 because of the change in the load impedance by the same factor.

The final result is that the predicted gain-bandwidth

MEASURED S-PARAMETERS

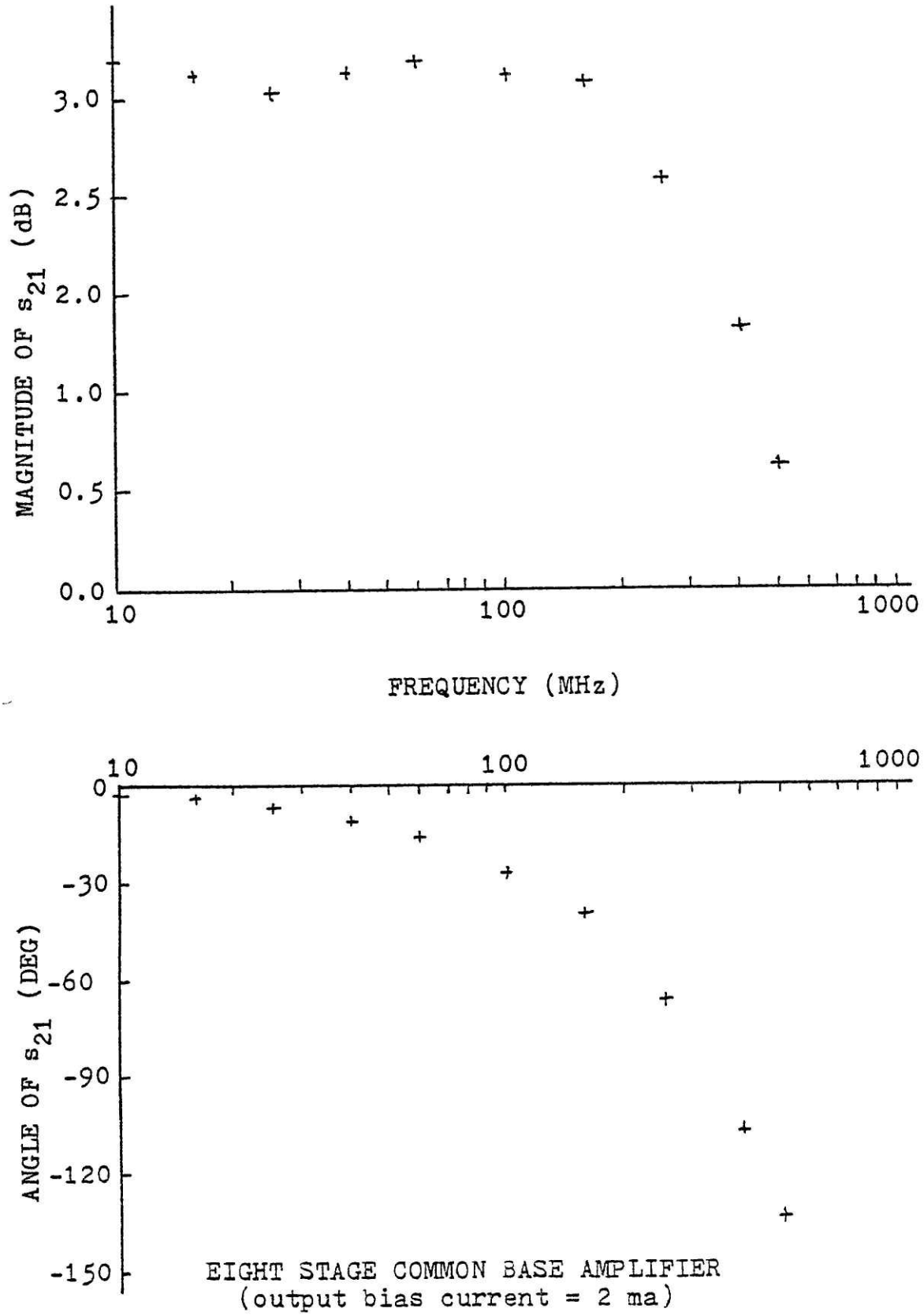
EIGHT STAGE COMMON BASE AMPLIFIER

(output bias current = 2 ma)

FREQUENCY MHz	S_{11} MAGNITUDE dB	S_{11} ANGLE DEG	S_{12} MAGNITUDE dB	S_{12} ANGLE DEG
10	-6.25	177.9	-61.1	76.2
15	-6.44	176.8	-57.6	81.4
25	-6.67	174.5	-53.2	86.0
40	-6.33	171.4	-49.0	88.9
60	-6.08	166.9	-45.3	91.2
100	-6.13	158.4	-40.1	93.2
150	-6.12	147.6	-35.8	92.9
250	-6.19	126.3	-29.7	87.2
400	-6.16	96.1	-23.5	70.3
500	-6.27	76.8	-20.6	56.6

FREQUENCY MHz	S_{21} MAGNITUDE dB	S_{21} ANGLE DEG	S_{22} MAGNITUDE dB	S_{22} ANGLE DEG
10	3.19	-2.8	.031	-2.2
15	3.14	-4.0	.022	-3.2
25	3.05	-6.8	.020	-5.4
40	3.15	-10.8	.033	-8.7
60	3.20	-16.1	.010	-13.0
100	3.13	-26.8	-.018	-21.7
150	3.00	-40.2	-.055	-32.5
250	2.60	-66.7	-.164	-54.7
400	1.84	-106.0	-.435	-88.8
500	1.12	-133.3	-.803	-113.6

FIG. 5.9



EIGHT STAGE COMMON BASE AMPLIFIER
(output bias current = 2 ma)

FIG. 5.10

product is,

$$GxBW = 1.0\ GHz \quad .$$

These two figures agree to within twenty percent which is quite good considering process tolerances, gain and bandwidth estimation techniques and the tendency toward underestimation in device modeling for circuit simulation.

FURTHER ANALYSIS

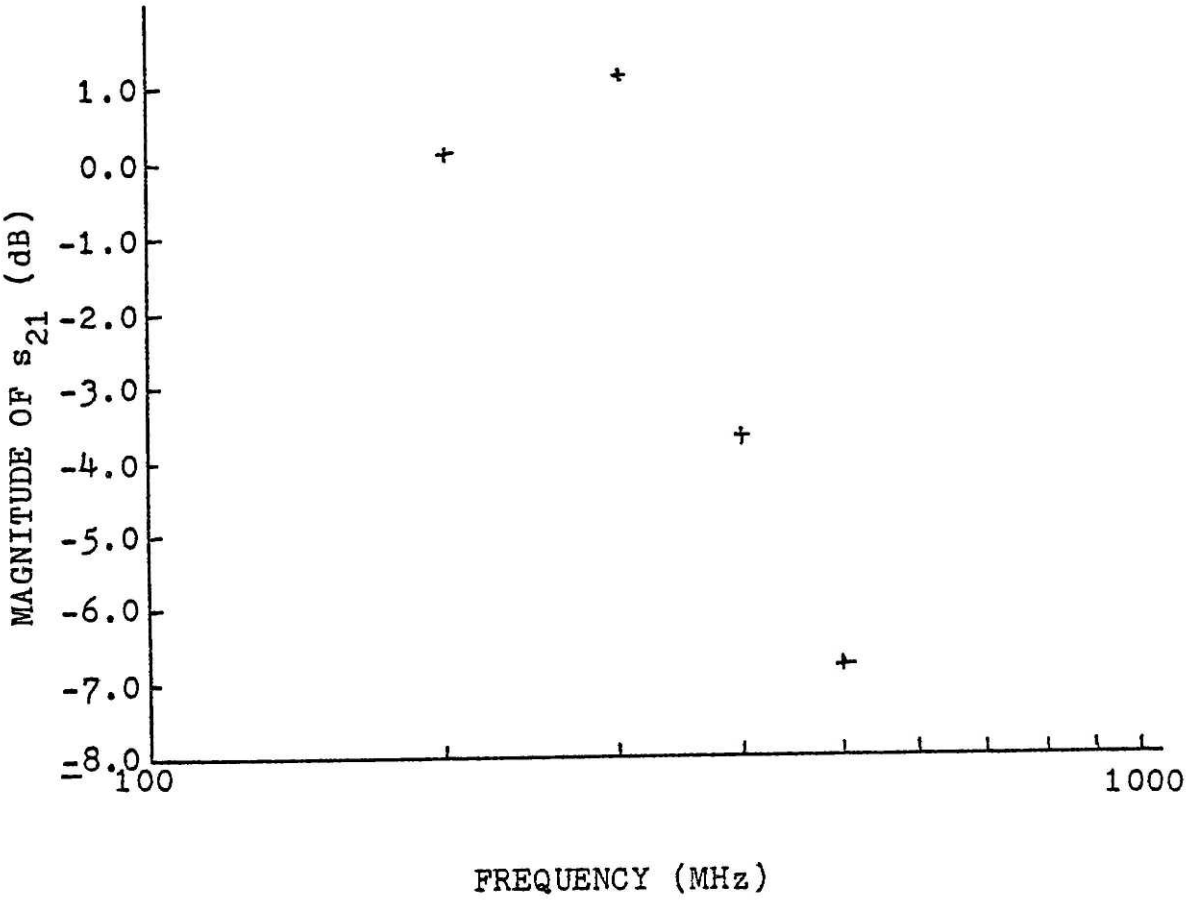
As a check on the work performed to this point, it was felt that a computer analysis of the multiple stage circuit using the single stage parameters would be useful. To carry this out, a circuit description of the eight stage common base amplifier tested in the previous section was entered into COMPACT, one of the circuit analysis programs in use at Lincoln Laboratory. The parameters for the individual stage were those measured for the single stage common base amplifier of the previous section. The transmission line physical dimensions were given for the input and output delay lines, allowing COMPACT to figure out the appropriate impedances, etc.

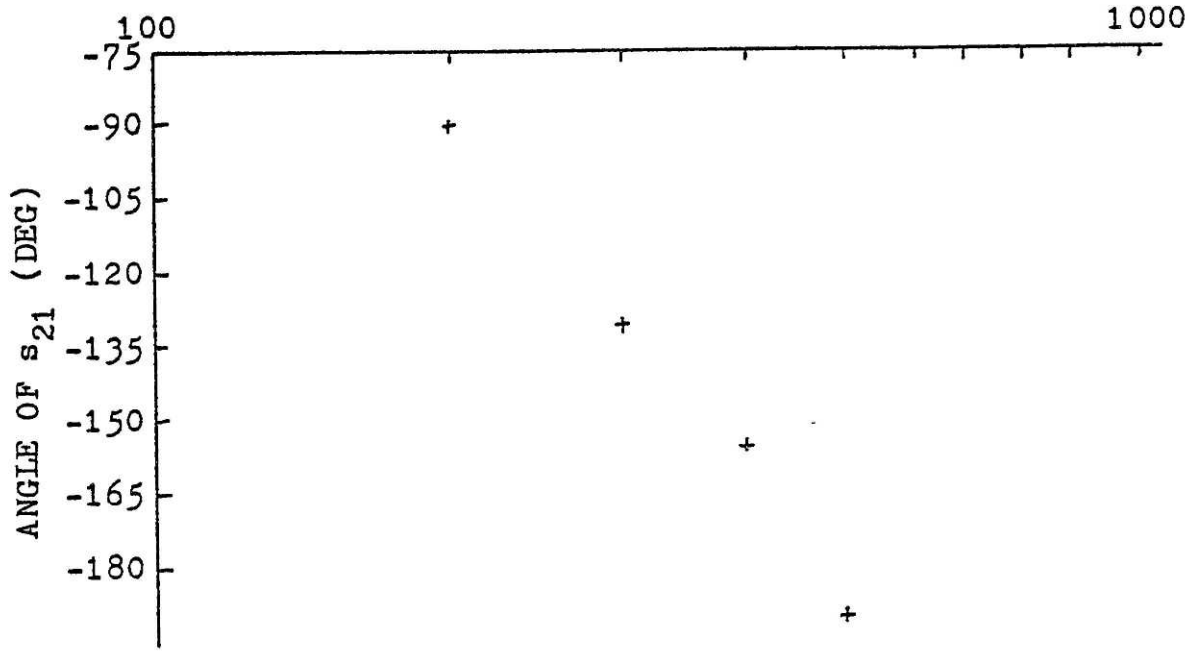
This was done at several frequencies, in an effort to determine the gain-bandwidth product, as had been done with the measured data. Representative of the results obtained are those shown in Figs. 6.1 and 6.2. As can be seen here, the bandwidth predicted by COMPACT was much smaller than that that was actually measured. In other words, using the values measured for the single stage amplifier, distributed operation is not to be expected.

These results are rather confusing, especially in light of the measured response. Further, in spite of circuit element and topology variations, these results seem to be fairly general. Although this has not been

```
>TRL AA MS 1.18 3.94 3.9 .059
.l
 TWO BB S1 50
 TRL CC MS .24 -3.94 3.9 .059
 TRL DD MS .24 1.97 3.9 .059
 TRL EE MS 1.18 1.97 3.9 .059
 CON AA T2 1 3
 CON BB T2 3 4
 CON CC T2 2 4
 CON AA T2 3 5
 CON BB T2 5 6
 CON CC T2 4 6
 CON AA T2 5 7
 CON CC T2 6 8
 CON BB T2 7 8
 CON AA T2 7 9
 CON CC T2 8 10
 CON BB T2 9 10
 CON EE T2 9 11
 CON DD T2 10 12
 DEF B1 T4 1 2 12 11
 CON B1 T4 1 2 3 4
 CON B1 T4 5 6 3 4
 DEF CC T2 1 6
 PRI CC S1 50
 END
 200 500 100
 END
 .48 65.1 1.075 -62.3 .0087 45.8 .995 -26.9
 .53 31.4 .924 -97 .011 32.4 .995 -26.9
 .562 5.7 .792 -109.1 .0126 21.9 .986 -53.6
 .575 -16.5 .68 -129.2 .0136 13.6 .983 -67.2
 END
 .01
 0 0 5 4
 END


>TRL AA MS 1.18 3.94 3.9 .059
.e
END OF MODS

                CIRCUIT OPTIMIZATION WITH  1 VARIABLES

 INITIAL CIRCUIT ANALYSIS

                    POLAR S-PARAMETERS IN   50.0 OHM SYSTEM
 FREQ.      S11              S21              S12              S22          S21     K
        (MAGN<ANGL) ( MAGN<ANGL) ( MAGN<ANGL) (MAGN<ANGL)    DB    FACT.

 200.00 0.78<  165  1.02< -90.3 0.008<  17.8 1.00< -125   0.14   0.14
 300.00 0.61<  159  1.15<-129.5 0.014<  -0.1 1.01< -126   1.20   0.17
 400.00 0.40<  173  0.66<-155.3 0.011< -24.3 1.00< -153  -3.57   0.53
 500.00 0.50< -156  0.45< 171.2 0.009< -46.8 1.00< -160  -6.95   0.74
```

FIG. 6.1





PREDICTED EIGHT STAGE COMMON BASE RESPONSE
USING SINGLE STAGE MEASURED S-PARAMETERS

FIG. 6.2

fully explained, the following is the most reasonable explanation presently available.

When the single stage amplifier (and all the other amplifiers, for that matter) was tested, it was assumed that the packaging of the test chip would not introduce appreciable effects. To a first approximation, this was certainly true for the magnitude of the s-parameters, but, due to the very high dielectric constant of the microstrip line connecting the chip to the test instrument, significant error was introduced in the measurement of the phase of the s-parameters. Because the size of the error was quite large, it is presumed that the prediction of the multiple stage operation from the measured single stage parameters will not be accurate.

Correcting such a problem turns out to be far from easy. In order to do so, the mounting block and connecting microstrip lines would need to be accounted for in the calibration process. Because of the limited storage capability of the 4051 mini-computer, this would require repeated bondings to the same circuit. It would also require a re-measurement of all the experimental data collected to this point. For these reasons, it was decided that further investigation would not be worth the required effort.

SUMMARY AND CONCLUSIONS

This thesis has attempted to demonstrate the feasibility of integrating a distributed amplifier. The fabricated parts were designed with the aid of computer circuit analysis and characterized in terms of their s-parameters. Experimental results confirm that distributed operation does occur, as predicted by theory. The important parameter here is the gain-bandwidth product. Attempts at further correlation between results and theory fail in a predictable manner.

Because the purpose of this dissertation is to demonstrate feasibility, no attempt was made to optimize this design for a specific application. Before this can be undertaken, however, a detailed analysis of the properties of the circuits presented here would be advantageous. Important properties of these amplifiers that have not been addressed include, linearity (total harmonic distortion), bias stability, temperature stability, effects of process variations, design flexibility, etc. In addition, the two transistor amplifier and a number of other variations should be investigated.

Hopefully, the miniaturization and the reduced design effort provided by circuit integration will make distributed amplifiers a viable design alternative in the near future.

APPENDIX A

COMPUTER PROGRAMS IN APL
FOR CALCULATING MICROSTRIP PARAMETERS

This appendix contains the major APL programs used to determine microstrip dimensions. Except for two supervisory programs, each one implements one of the equations presented by Wheeler. A brief description of each would be (see text for variable definition):

STRIPTABLE - user interface program, prompts supplied for all necessary inputs, outputs a table of stripline parameters.

DESIGN - supervisory program, input is an ordered vector, h t w z, one of which is zero, outputs same ordered vector with missing value replaced with computed value.

EWHR - calculates w'/h given an ordered vector, z k, prompts supplied if only z is given.

DWTR - calculates $\Delta w/t$ given an ordered vector, h t w, prompts supplied if input missing.

DEW - calculates $\Delta w'$ given an ordered vector, Δw k, prompts supplied if only Δw given.

R - calculates z given an ordered vector, w'/h k, prompts supplied if only w'/h is given.

R1 - calculates z for the no dielectric case given w'/h.

EWHR1 - calculates w'/h for the no dielectric case given z.

```
∇ STRIPTABLE;Z;H;T;W;K;J;M;ANS;H1;T1;W1;Z1
[1]   'THIS PROGRAM HAS BEEN FORMULATED TO HELP THE DESIGNER OF MICROSTRIP'
[2]   '(A STRIP ON A DIELECTRIC SHEET ON A PLANE) TRANSMISSION LINE.  IT WILL'
[3]   'CALCULATE AND TABULATE ONE OF FOUR DESIGN PARAMETERS FOR A RANGE OF'
[4]   'THE OTHER THREE.  THE DESIGN PARAMETERS ARE Z, H, T, AND W, WHERE Z IS'
[5]   'THE CHARACTERISTIC IMPEDANCE OF THE LINE, H IS THE HEIGHT OF THE DIELEC-'
[6]   'TRIC, T IS THE THICKNESS OF THE LINE, AND W IS THE WIDTH OF THE LINE.'
[7]   'THE UNITS OF Z ARE OHMS, AND THE UNITS OF THE REMAINING PARAMETERS ARE'
[8]   'VARIABLE AS LONG AS THEY ARE THE SAME FOR ALL DIMENSIONS.'
[9]   ''
[10]  'PLEASE ENTER THE VALUE OF K, THE DIELECTRIC CONSTANT OF THE INSULATING'
[11]  'MEDIUM.  THE PROPER FORMAT IS - K=VALUE.'
[12]  K←⍎2↓⍞
[13]  ''
[14]  'PLEASE ENTER THREE OF THE FOUR DESIGN PARAMETERS, Z, H, T, OR W.  THE'
[15]  'PROPER FORMAT IS - DESIGN_VARIABLE=LOWER_BOUND,UPPER_BOUND,INCREMENT'
[16]  ''
[17]  '                    EXAMPLE:'
[18]  '                                  Z=25,100,5'
[19]  Z←W←T←H←0,0,1
[20]  ANS← 1 4 ⍴0
[21]  M←0
[22]  L1:''
[23]  →((+/×(Z[1],W[1],H[1],T[1]))=3)/L6
[24]  M←⍞
[25]  →(M[1]='Z','W','H','T')/L2,L3,L4,L5
[26]  L2:Z←⍎2↓M
[27]  →L1
[28]  L3:W←⍎2↓M
[29]  →L1
[30]  L4:H←⍎2↓M
[31]  →L1
[32]  L5:T←⍎2↓M
[33]  →L1
[34]  L6:M←0
[35]  H1←H[1]
[36]  T1←T[1]
[37]  W1←W[1]
[38]  Z1←Z[1]
[39]  L7:ANS←ANS,[1] DESIGN H[1],T[1],W[1],Z[1]
[40]  →(Z[2]≥Z[1]←Z[1]+Z[3])/L7
[41]  Z[1]←Z1
[42]  →(W[2]≥W[1]←W[1]+W[3])/L7
```

```
[43]   W[1]←W1
[44]   →(T[2]≥T[1]←T[1]+T[3])/L7
[45]   T[1]←T1
[46]   →(H[2]≥H[1]←H[1]+H[3])/L7
[47]   ''
[48]   ''
[49]   '      Z           W           T           H'
[50]   '*----------*----------*----------*----------*'
[51]   □← 10 4 ▼ANS← 1 0 ↓ANS
       ∇
```

```
       ∇ ANS←DESIGN HTWZ;M;T1;T2;T3;T4;H;T;W;Z
[1]      H←HTWZ[1]
[2]      T←HTWZ[2]
[3]      W←HTWZ[3]
[4]      Z←HTWZ[4]
[5]    L6:→((Z,H,T,W)=0)/L8,L9,L10,L11
[6]    L8:T1←T×DWTR H,T,W
[7]      T1←W÷DEN T1,K
[8]      T1←R(T1÷H),K
[9]      ANS←T1,W,T,H
[10]     →0
[11]   L9:T1←EWHR Z,K
[12]     H←2×T
[13]     T4←2÷1+1÷K
[14]   L12:T2←(W÷T×(DWTR H,T,W)×T4)÷T1
[15]     →((|H-T2)<1E¯6)/L14
[16]     H←(H+T2)÷2
[17]     →L12
[18]     ANS←Z,W,T,H
[19]     →0
[20]   L10:T1←(2÷1+1÷K)×(H×EWHR Z,K)-W
[21]     T←H
[22]   L13:T2←T1÷DWTR H,T,W
[23]     →((|T-T2)<0.001)/L16
[24]     T←(T+T2)÷2
[25]     →L13
[26]     ANS←Z,W,T,H
[27]     →0
[28]   L11:T1←(H×EWHR Z,K)-(DEN(T×DWTR H,T,W),K)
[29]     ANS←Z,T1,T,H
       ∇
```

```
    ∇ Z←EWHR R;K
[1]   →((ρR)=2)/L1
[2]   ⍞←'PLEASE TYPE IN THE VALUE OF THE DIELECTRIC CONSTANT, K'
[3]   K←⍞
[4]   Z←(*R×((K+1)*0.5)÷42.4)-1
[5]   Z←8×((((Z×7+4÷K)÷11)+(1+1÷K)÷0.81)*0.5)÷Z
[6]   ⍞←'THE EFFECTIVE WIDTH TO HEIGHT RATIO FOR R = ',(▼R),' AND K = ',(▼K),' IS ',▼Z
[7]   Z←ρ0
[8]   →0
[9]  L1:K←R[2]
[10]  R←R[1]
[11]  Z←(*R×((K+1)*0.5)÷42.4)-1
[12]  Z←8×((((Z×7+4÷K)÷11)+(1+1÷K)÷0.81)*0.5)÷Z
    ∇
```

```
    ∇ Z←DWTR HTW
[1]   →((ρHTW)=3)/L1
[2]   ⍞←'TYPE IN THE DIMENSIONS H, T, AND W, AS A VECTOR: D1 D2 D3'
[3]   HTW←⍞
[4]   Z←(⊛4×(*1)÷(((HTW[2]÷HTW[1])*2)+((1÷(01)×1.1+HTW[3]÷HTW[2])*2))*0.5)÷(01)
[5]   ⍞←'THE CHANGE IN WIDTH DUE TO FINITE STRIP THICKNESS FOR H = ',(▼HTW[1]),', T = ',(▼HTW[2]),','
[6]   ⍞←'AND W = ',(▼HTW[3]),' IS ',▼Z×HTW[2]
[7]   →ρZ←ρ0
[8]  L1:Z←(⊛4×(*1)÷(((HTW[2]÷HTW[1])*2)+((1÷(01)×1.1+HTW[3]÷HTW[2])*2))*0.5)÷(01)
    ∇
```

```
    ∇ Z←DFW DW
[1]   →((ρDW)=2)/L1
[2]   ⍞←'TYPE IN THE DIELECTRIC CONSTANT, K'
[3]   K←⍞
[4]   ⍞←'THE CHANGE IN THE EFFECTIVE WIDTH DUE TO FINITE STRIP THICKNESS'
[5]   ⍞←'IS ',▼Z←(1+1÷K)×DW÷2
[6]   →ρZ←ρ0
[7]  L1:Z←DW[1]×(1+1÷K←DW[2])÷2
    ∇
```

```
    ∇ Z←R EWHR;K
[1]   →((ρEWHR)=2)/L1
[2]   []←'PLEASE TYPE IN THE VALUE OF THE DIELECTRIC CONSTANT, K'
[3]   K←[]
[4]   Z←(4÷EWHR)×(14+8÷K)÷11
[5]   Z←(42.4×⍟1+(4÷EWHR)×Z+((Z*2)+(1+1÷K)×((○1)*2)÷2)*0.5)÷(K+1)*0.5
[6]   []←'THE CHARACTERISTIC IMPEDANCE FOR EWHR = ',(▼EWHR),' AND K = ',(▼K),' IS ',▼Z
[7]   →ρZ←ρ0
[8]  L1:Z←(4÷EWHR←EWHR[1])×(14+8÷K←EWHR[2])÷11
[9]   Z←(42.4×⍟1+(4÷EWHR)×Z+((Z*2)+(1+1÷K)×((○1)*2)÷2)*0.5)÷(K+1)*0.5
    ∇
```

```
    ∇ Z←R1 EWTOH
[1]   →((ρEWTOH)=2)/L1
[2]   Z←8÷EWTOH
[3]   Z←30×⍟1+0.5×Z×Z+((Z*2)+(○1)*2)*0.5
[4]   []←'THE CHARACTERISTIC IMPEDANCE FOR W''/H = ',(▼EWTOH),' IS ',▼Z
[5]   →ρZ←ρ0
[6]  L1:Z←30×⍟1+0.5×Z×Z+(((Z←(8÷EWTOH←EWTOH[1]))*2)+(○1)*2)*0.5
    ∇
```

```
    ∇ Z←EWHR1 R1
[1]   →((ρR1)=2)/L1
[2]   Z←8×((((*R1÷30)-1)+0.25×(○1)*2)*0.5)÷(*R1÷30)-1
[3]   []←'THE EFFECTIVE WIDTH TO HEIGHT RATIO FOR R1 = ',(▼R1),' IS ',▼Z
[4]   Z←ρ0
[5]   →0
[6]  L1:Z←8×((((*R1÷30)-1)+0.25×(○1)*2)*0.5)÷(*(R1←R1[1])÷30)-1
    ∇
```

```
      STRIPTABLE
THIS PROGRAM HAS BEEN FORMULATED TO HELP THE DESIGNER OF MICROSTRIP
(A STRIP ON A DIELECTRIC SHEET ON A PLANE) TRANSMISSION LINE.  IT WILL
CALCULATE AND TABULATE ONE OF FOUR DESIGN PARAMETERS FOR A RANGE OF
THE OTHER THREE.  THE DESIGN PARAMETERS ARE Z, H, T, AND W, WHERE Z IS
THE CHARACTERISTIC IMPEDANCE OF THE LINE, H IS THE HEIGHT OF THE DIELEC-
TRIC, T IS THE THICKNESS OF THE LINE, AND W IS THE WIDTH OF THE LINE.
THE UNITS OF Z ARE OHMS, AND THE UNITS OF THE REMAINING PARAMETERS ARE
VARIABLE AS LONG AS THEY ARE THE SAME FOR ALL DIMENSIONS.

PLEASE ENTER THE VALUE OF K, THE DIELECTRIC CONSTANT OF THE INSULATING
MEDIUM.  THE PROPER FORMAT IS - K=VALUE.
K=4

PLEASE ENTER THREE OF THE FOUR DESIGN PARAMETERS, Z, H, T, OR W.  THE
PROPER FORMAT IS - DESIGN_VARIABLE=LOWER_BOUND,UPPER_BOUND,INCREMENT

                    EXAMPLE:
                                  Z=25,100,5

Z=5,50,5

H=.8,1.2,.2

T=.8,1.2,.2


     Z          W          T          H
*----------*----------*----------*----------*
    5.0000    27.7882     .8000      .8000
   10.0000    12.8158     .8000      .8000
   15.0000     7.8840     .8000      .8000
   20.0000     5.4551     .8000      .8000
   25.0000     4.0216     .8000      .8000
   30.0000     3.0817     .8000      .8000
   35.0000     2.4209     .8000      .8000
   40.0000     1.9324     .8000      .8000
   45.0000     1.5576     .8000      .8000
   50.0000     1.2614     .8000      .8000
```

5.0000	27.7364	1.0000	.8000
10.0000	12.7640	1.0000	.8000
15.0000	7.8323	1.0000	.8000
20.0000	5.4033	1.0000	.8000
25.0000	3.9698	1.0000	.8000
30.0000	3.0299	1.0000	.8000
35.0000	2.3691	1.0000	.8000
40.0000	1.8806	1.0000	.8000
45.0000	1.5058	1.0000	.8000
50.0000	1.2097	1.0000	.8000
5.0000	27.6930	1.2000	.8000
10.0000	12.7206	1.2000	.8000
15.0000	7.7889	1.2000	.8000
20.0000	5.3599	1.2000	.8000
25.0000	3.9265	1.2000	.8000
30.0000	2.9866	1.2000	.8000
35.0000	2.3257	1.2000	.8000
40.0000	1.8373	1.2000	.8000
45.0000	1.4624	1.2000	.8000
50.0000	1.1663	1.2000	.8000
5.0000	34.7964	.8000	1.0000
10.0000	16.0809	.8000	1.0000
15.0000	9.9163	.8000	1.0000
20.0000	6.8801	.8000	1.0000
25.0000	5.0882	.8000	1.0000
30.0000	3.9133	.8000	1.0000
35.0000	3.0873	.8000	1.0000
40.0000	2.4767	.8000	1.0000
45.0000	2.0082	.8000	1.0000
50.0000	1.6380	.8000	1.0000
5.0000	34.7352	1.0000	1.0000
10.0000	16.0197	1.0000	1.0000
15.0000	9.8550	1.0000	1.0000
20.0000	6.8188	1.0000	1.0000
25.0000	5.0270	1.0000	1.0000
30.0000	3.8521	1.0000	1.0000
35.0000	3.0261	1.0000	1.0000
40.0000	2.4155	1.0000	1.0000
45.0000	1.9469	1.0000	1.0000
50.0000	1.5768	1.0000	1.0000

5.0000	34.6825	1.2000	1.0000
10.0000	15.9670	1.2000	1.0000
15.0000	9.8024	1.2000	1.0000
20.0000	6.7662	1.2000	1.0000
25.0000	4.9743	1.2000	1.0000
30.0000	3.7995	1.2000	1.0000
35.0000	2.9734	1.2000	1.0000
40.0000	2.3628	1.2000	1.0000
45.0000	1.8943	1.2000	1.0000
50.0000	1.5241	1.2000	1.0000
5.0000	41.8117	.8000	1.2000
10.0000	19.3531	.8000	1.2000
15.0000	11.9556	.8000	1.2000
20.0000	8.3121	.8000	1.2000
25.0000	6.1619	.8000	1.2000
30.0000	4.7521	.8000	1.2000
35.0000	3.7608	.8000	1.2000
40.0000	3.0281	.8000	1.2000
45.0000	2.4658	.8000	1.2000
50.0000	2.0217	.8000	1.2000
5.0000	41.7426	1.0000	1.2000
10.0000	19.2840	1.0000	1.2000
15.0000	11.8865	1.0000	1.2000
20.0000	8.2430	1.0000	1.2000
25.0000	6.0928	1.0000	1.2000
30.0000	4.6830	1.0000	1.2000
35.0000	3.6917	1.0000	1.2000
40.0000	2.9590	1.0000	1.2000
45.0000	2.3967	1.0000	1.2000
50.0000	1.9526	1.0000	1.2000
5.0000	41.6822	1.2000	1.2000
10.0000	19.2236	1.2000	1.2000
15.0000	11.8261	1.2000	1.2000
20.0000	8.1826	1.2000	1.2000
25.0000	6.0324	1.2000	1.2000
30.0000	4.6226	1.2000	1.2000
35.0000	3.6313	1.2000	1.2000
40.0000	2.8986	1.2000	1.2000
45.0000	2.3363	1.2000	1.2000
50.0000	1.8922	1.2000	1.2000

APPENDIX B

COMPUTER PREDICTED STEP RESPONSE

COMPUTER PREDICTED STEP RESPONSE PARAMETERS

CIRCUIT TYPE	NUMBER OF STAGES	INPUT AMPLITUDE (volts)	OUTPUT AMPLITUDE (volts)	INITIAL SLOPE (v/nsec)	BIAS CURRENT /STAGE (ma)	Z_o (Ω)
common base	1	.15	.02	.029	.59	25
common base	2	.15	.03	.081	.5	25
common base	5	.1	.1	.17	.049	25
common base	10	.1	.14	.22	.045	250
common base	20	.05	.14	.16	.86	50
common emitter	1	.1	.02	.029	6.0	25
common emitter	1	.1	.036	.025	8.0	25
common emitter	20	.05	.04	.054	1.2	50
two transistor	5	.2	.18	.13	.078	50
two transistor	20	.05	.035	.05	4.2	50
two transistor	20	.1	.2	.044	2.0	50

COMPUTER PREDICTED STEP RESPONSE PARAMETERS

CIRCUIT TYPE	NUMBER OF STAGES	TIME CONSTANT (nsec)	G_o	G_p	GxBW (MHz)
common base	1	.7	.13	.017	3.8
common base	2	.37	.2	.04	17.2
common base	5	.6	1.0	1.0	265
common base	10	.65	1.4	2.0	490
common base	20	.9	2.8	7.8	1390
common emitter	1	.68	.2	.04	9.4
common emitter	1	1.44	.36	.13	14.3
common emitter	20	.74	.8	.64	140
two transistor	5	1.4	.9	.81	92
two transistor	20	.7	.7	.49	111
two transistor	20	4.5	2.0	4.0	140

APPENDIX C

MEASURED S-PARAMETERS

MEASURED S-PARAMETERS

SINGLE STAGE COMMON BASE AMPLIFIER

(output bias current = 1 ma)

	S_{11}		S_{12}	
FREQUENCY MHz	MAGNITUDE dB	ANGLE DEG	MAGNITUDE dB	ANGLE DEG
10	-27.8	144.9	-66.4	64.5
15	-28.3	98.4	-63.3	72.8
25	-24.0	69.1	-58.9	76.7
40	-20.1	94.8	-54.7	76.2
60	-16.2	95.2	-51.2	73.3
100	-12.9	71.1	-47.0	66.4
150	-9.9	55.0	-43.9	57.7
250	-7.1	26.1	-40.8	42.7
400	-5.4	-7.1	-38.6	25.1
500	-4.9	-26.4	-37.8	15.5

	S_{21}		S_{22}	
FREQUENCY MHz	MAGNITUDE dB	ANGLE DEG	MAGNITUDE dB	ANGLE DEG
10	0.05	-3.1	0.04	-1.2
15	-0.21	-4.9	0.03	-2.0
25	-0.36	-8.1	0.01	-3.3
40	-0.06	-12.4	0.04	-5.3
60	0.17	-18.9	0.03	-8.0
100	-0.25	-31.0	0.02	-13.5
150	-0.66	-45.5	0.02	-20.1
250	-1.85	-71.3	-0.02	-33.7
400	-3.58	-103.0	-0.06	-54.0
500	-4.65	-122.5	-0.08	-66.6

MEASURED S-PARAMETERS

SINGLE STAGE COMMON BASE AMPLIFIER

(output bias current = 2 ma)

	S_{11}		S_{12}	
FREQUENCY MHz	MAGNITUDE dB	ANGLE DEG	MAGNITUDE dB	ANGLE DEG
10	-10.2	171.7	-65.4	66.4
15	-10.4	167.3	-62.0	72.4
25	-10.4	158.9	-57.2	75.8
40	-10.0	147.6	-53.1	75.0
60	-9.4	133.3	-49.8	71.3
100	-8.6	106.9	-45.7	63.7
150	-7.5	80.5	-42.8	54.1
250	-6.0	42.0	-39.9	39.0
400	-5.0	2.1	-37.8	21.6
500	-4.7	-19.4	-37.1	12.3

	S_{21}		S_{22}	
FREQUENCY MHz	MAGNITUDE dB	ANGLE DEG	MAGNITUDE dB	ANGLE DEG
10	2.04	-3.4	0.04	-1.2
15	1.99	-5.2	0.02	-1.9
25	1.91	-8.7	0.01	-3.2
40	1.93	-13.6	0.04	-5.4
60	1.87	-20.4	0.02	-8.0
100	1.50	-33.3	0.01	-13.4
150	0.91	-48.6	0.01	-20.2
250	-0.47	-75.2	-0.03	-33.7
400	-2.46	-107.9	-0.07	-54.0
500	-3.68	-128.1	-0.10	-66.7

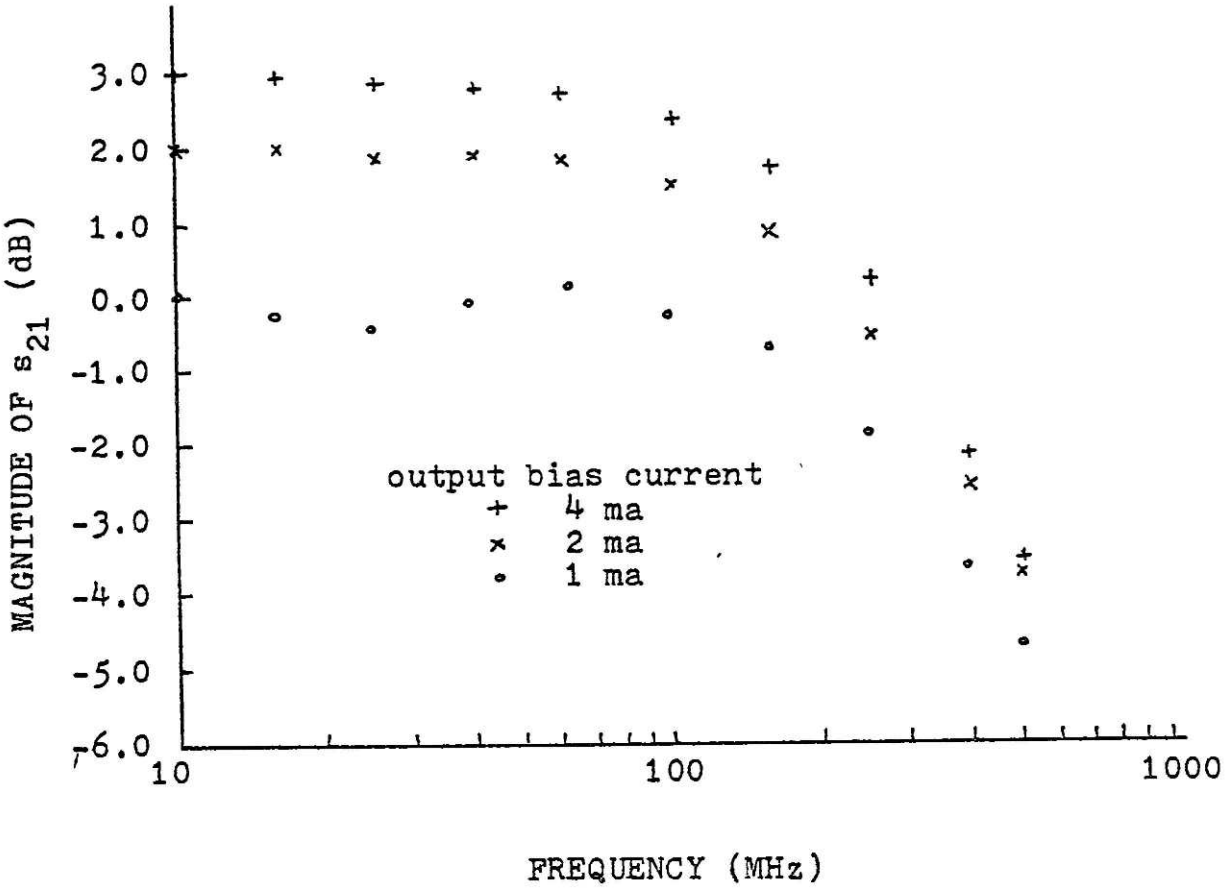
MEASURED S-PARAMETERS

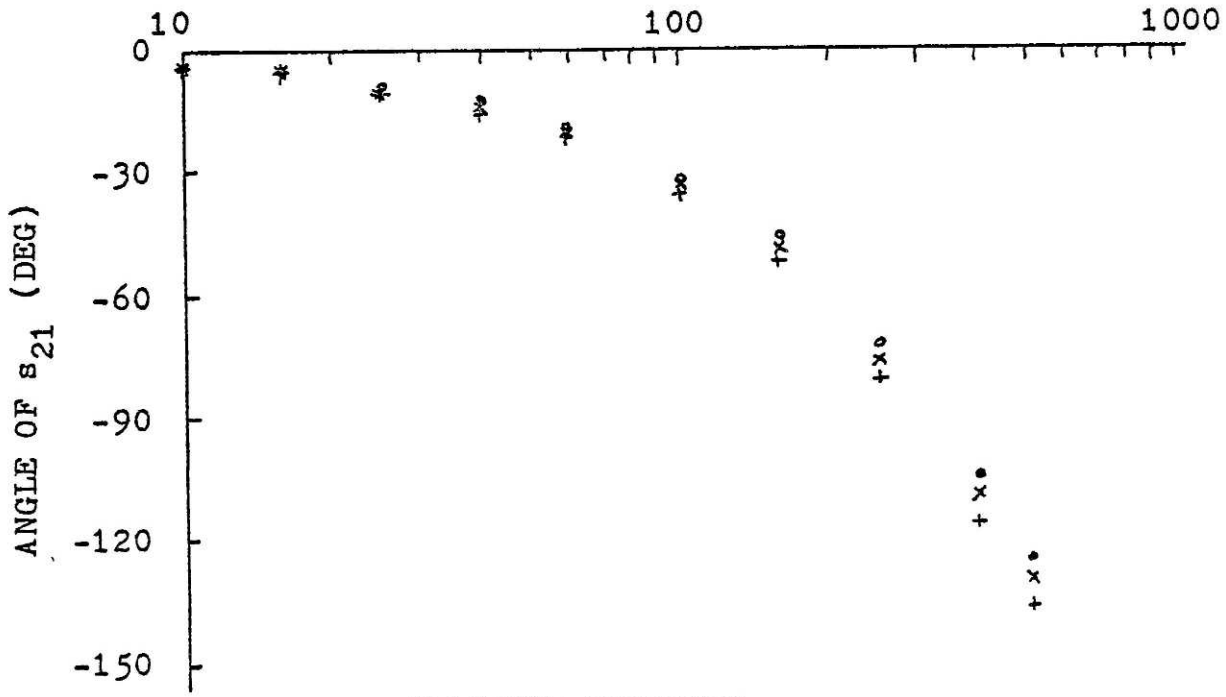
SINGLE STAGE COMMON BASE AMPLIFIER

(output bias current = 4 ma)

FREQUENCY MHz	S_{11} MAGNITUDE dB	S_{11} ANGLE DEG	S_{12} MAGNITUDE dB	S_{12} ANGLE DEG
10	-6.72	172.9	-64.7	61.4
15	-6.75	169.5	-60.5	72.0
25	-6.73	162.6	-56.1	74.4
40	-6.66	152.5	-51.8	73.1
60	-6.52	139.4	-48.5	69.6
100	-6.23	115.1	-44.6	61.7
150	-5.74	88.8	-41.7	52.0
250	-4.97	48.4	-38.9	36.6
400	-4.49	5.1	-37.0	18.3
500	-4.45	-17.5	-36.4	8.5

FREQUENCY MHz	S_{21} MAGNITUDE dB	S_{21} ANGLE DEG	S_{22} MAGNITUDE dB	S_{22} ANGLE DEG
10	2.98	-3.7	0.04	-1.2
15	2.96	-5.5	0.02	-2.0
25	2.91	-9.2	0.01	-3.2
40	2.86	-14.5	0.03	-5.4
60	2.74	-21.5	0.02	-8.1
100	2.36	-35.2	0.01	-13.5
150	1.77	-51.4	0.00	-20.3
250	0.27	-80.2	-0.04	-33.9
400	-2.07	-115.5	-0.09	-54.2
500	-3.54	-136.3	-0.12	-66.8





MEASURED RESPONSE
SINGLE STAGE COMMON BASE AMPLIFIER

MEASURED S-PARAMETERS

EIGHT STAGE COMMON BASE AMPLIFIER

(output bias current = 2 ma)

FREQUENCY MHz	S_{11} MAGNITUDE dB	S_{11} ANGLE DEG	S_{12} MAGNITUDE dB	S_{12} ANGLE DEG
10	-6.25	177.9	-61.1	76.2
15	-6.44	176.8	-57.6	81.4
25	-6.67	174.5	-53.2	86.0
40	-6.33	171.4	-49.0	88.9
60	-6.08	166.9	-45.3	91.2
100	-6.13	158.4	-40.1	93.2
150	-6.12	147.6	-35.8	92.9
250	-6.19	126.3	-29.7	87.2
400	-6.16	96.1	-23.5	70.3
500	-6.27	76.8	-20.6	56.6

FREQUENCY MHz	S_{21} MAGNITUDE dB	S_{21} ANGLE DEG	S_{22} MAGNITUDE dB	S_{22} ANGLE DEG
10	3.19	-2.8	.031	-2.2
15	3.14	-4.0	.022	-3.2
25	3.05	-6.8	.020	-5.4
40	3.15	-10.8	.033	-8.7
60	3.20	-16.1	.010	-13.0
100	3.13	-26.8	-.018	-21.7
150	3.00	-40.2	-.055	-32.5
250	2.60	-66.7	-.164	-54.7
400	1.84	-106.0	-.435	-88.8
500	1.12	-133.3	-.803	-113.6

MEASURED S-PARAMETERS

EIGHT STAGE COMMON BASE AMPLIFIER

(output bias current = 6 ma)

FREQUENCY MHz	S_{11} MAGNITUDE dB	S_{11} ANGLE DEG	S_{12} MAGNITUDE dB	S_{12} ANGLE DEG
25	-2.28	174.5	-52.0	85.8
40	-2.28	171.2	-47.9	88.8
60	-2.29	166.9	-44.1	90.6
100	-2.32	158.4	-39.1	92.7
150	-2.35	147.5	-34.7	92.3
250	-2.48	126.3	-28.6	85.9
400	-2.69	95.7	-22.3	67.6
500	-2.90	75.8	-19.4	52.7

FREQUENCY MHz	S_{21} MAGNITUDE dB	S_{21} ANGLE DEG	S_{22} MAGNITUDE dB	S_{22} ANGLE DEG
25	4.69	-6.7	0.02	-5.5
40	4.67	-10.5	0.03	-8.7
60	4.66	-15.8	0.01	-13.3
100	4.60	-26.2	-0.01	-21.8
150	4.48	-39.4	-0.04	-32.8
250	4.16	-65.4	-0.15	-55.3
400	3.48	-104.3	-0.39	-90.1
500	2.86	-131.7	-0.76	-115.5

MEASURED S-PARAMETERS

EIGHT STAGE COMMON BASE AMPLIFIER

(output bias current = 10 ma)

	S_{11}		S_{12}	
FREQUENCY MHz	MAGNITUDE dB	ANGLE DEG	MAGNITUDE dB	ANGLE DEG
25	-1.63	174.5	-51.8	85.3
40	-1.62	171.3	-48.1	88.0
60	-1.62	167.0	-44.1	90.8
100	-1.65	158.5	-38.9	93.5
150	-1.70	149.0	-34.6	93.3
250	-1.81	127.1	-28.4	89.8
400	-1.94	96.0	-22.1	74.1
500	-2.18	76.3	-19.1	59.8

	S_{21}		S_{22}	
FREQUENCY MHz	MAGNITUDE dB	ANGLE DEG	MAGNITUDE dB	ANGLE DEG
25	4.98	-6.1	0.02	-5.5
40	4.97	-9.7	0.01	-8.9
60	4.96	-14.7	-0.01	-13.4
100	4.91	-24.6	-0.03	-22.2
150	4.76	-37.1	-0.08	-33.0
250	4.46	-61.5	-0.17	-55.2
400	3.94	-98.8	-0.43	-91.1
500	3.18	-124.6	-0.79	-116.9

MEASURED S-PARAMETERS

EIGHT STAGE COMMON BASE AMPLIFIER

(output bias current = 15 ma)

FREQUENCY MHz	S_{11} MAGNITUDE dB	S_{11} ANGLE DEG	S_{12} MAGNITUDE dB	S_{12} ANGLE DEG
25	-1.29	174.4	-51.5	84.5
40	-1.28	171.2	-47.8	87.3
60	-1.28	167.0	-43.7	90.2
100	-1.31	158.6	-38.6	92.8
150	-1.36	148.2	-34.3	93.5
250	-1.45	127.3	-28.1	88.3
400	-1.56	95.9	-21.7	73.1
500	-1.83	75.8	-18.8	58.3

FREQUENCY MHz	S_{21} MAGNITUDE dB	S_{21} ANGLE DEG	S_{22} MAGNITUDE dB	S_{22} ANGLE DEG
25	5.14	-6.1	0.02	-5.5
40	5.12	-9.8	0.01	-9.0
60	5.11	-14.8	-0.01	-13.6
100	5.06	-24.8	-0.03	-22.4
150	4.93	-37.5	-0.08	-33.4
250	4.68	-62.3	-0.18	-55.8
400	4.18	-101.0	-0.46	-92.2
500	3.38	-127.6	-0.86	-118.5

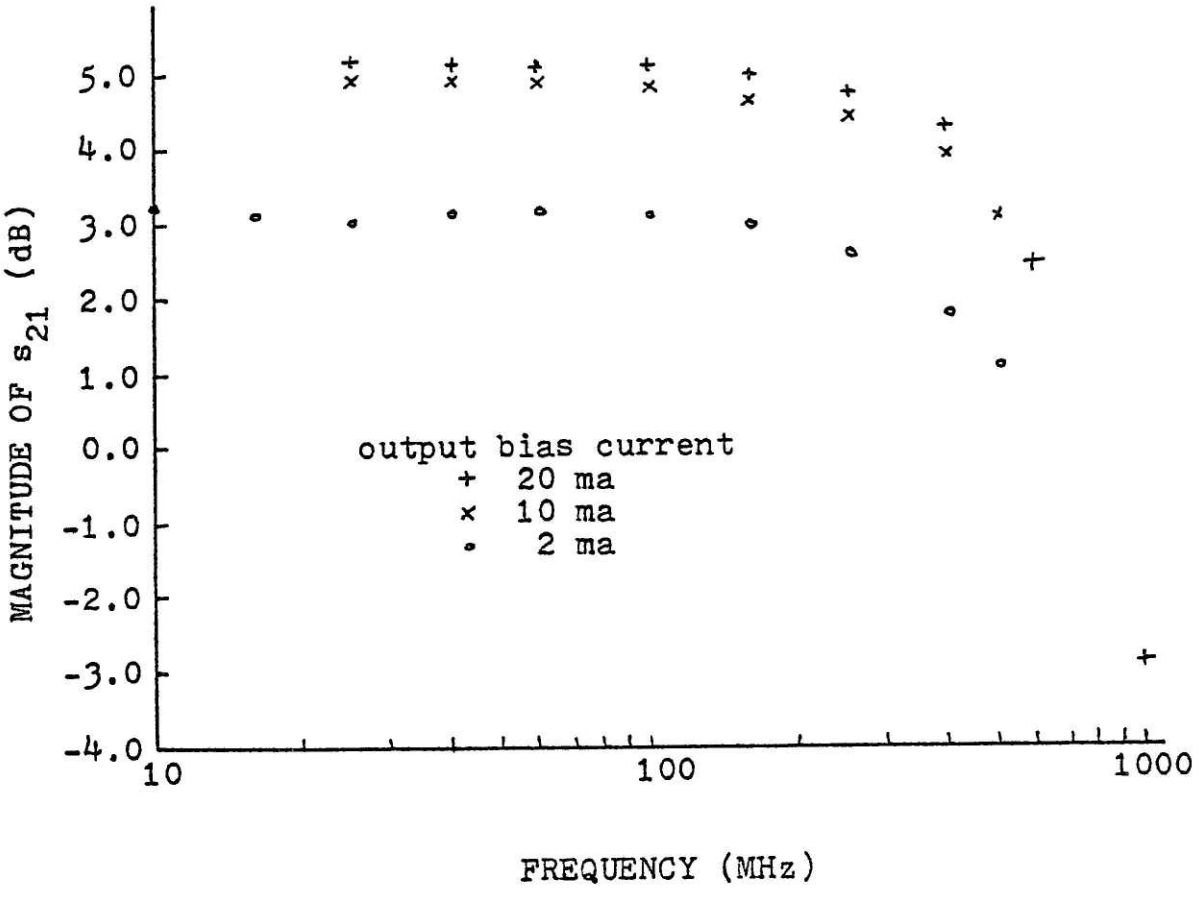
MEASURED S-PARAMETERS

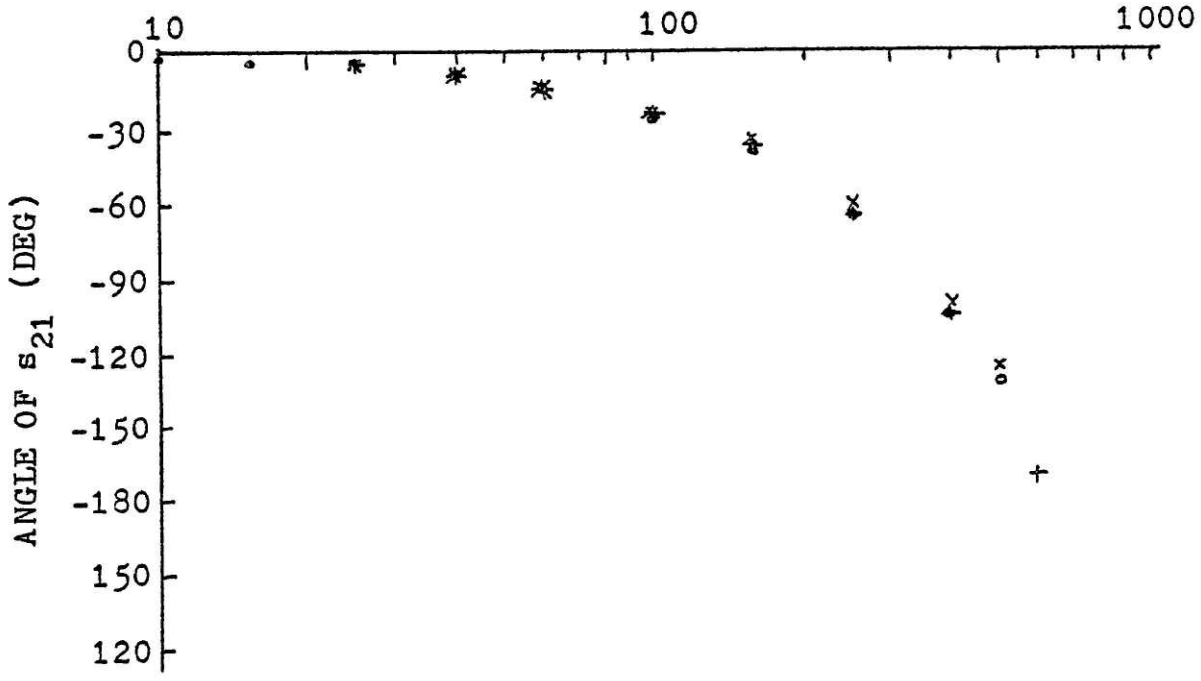
EIGHT STAGE COMMON BASE AMPLIFIER

(output bias current = 20 ma)

	S_{11}		S_{12}	
FREQUENCY MHz	MAGNITUDE dB	ANGLE DEG	MAGNITUDE dB	ANGLE DEG
25	-1.12	174.5	-51.1	84.7
40	-1.13	171.3	-47.3	87.2
60	-1.12	167.0	-43.3	89.7
100	-1.15	158.5	-38.3	92.2
150	-1.19	148.2	-34.0	92.8
250	-1.26	127.1	-27.8	87.6
400	-1.40	95.3	-21.4	71.9
600	-2.13	54.4	-16.5	32.3
1000	-4.86	-11.6	-12.3	-28.0

	S_{21}		S_{22}	
FREQUENCY MHz	MAGNITUDE dB	ANGLE DEG	MAGNITUDE dB	ANGLE DEG
25	5.20	-6.2	.011	-5.6
40	5.19	-9.9	.003	-9.1
60	5.18	-14.9	-.011	-13.8
100	5.15	-25.2	-.043	-22.7
150	5.03	-38.1	-.082	-33.8
250	4.80	-63.5	-.185	-56.4
400	4.28	-103.5	-.507	-93.6
600	2.52	-170.9	-1.702	-147.4
1000	-2.78	68.8	-5.352	104.3





MEASURED RESPONSE
EIGHT STAGE COMMON BASE AMPLIFIER

MEASURED S-PARAMETERS

SINGLE STAGE COMMON EMITTER AMPLIFIER

(output bias current = .2 ma)

	S_{11}		S_{12}	
FREQUENCY MHz	MAGNITUDE dB	ANGLE DEG	MAGNITUDE dB	ANGLE DEG
1	-1.52	-0.3	-76.2	56.3
1.5	-1.52	-0.5	-81.1	20.2
2.5	-1.52	-0.9	-76.8	36.8
4	-1.52	-1.5	-75.8	52.9
6	-1.53	-2.3	-73.0	58.9
10	-1.54	-3.7	-68.5	69.3
15	-1.57	-5.5	-66.1	70.2
25	-1.69	-8.9	-62.4	70.8
40	-1.98	-13.5	-58.6	66.8
60	-2.43	-18.6	-55.8	60.8
100	-3.26	-26.1	-53.0	54.5

	S_{21}		S_{22}	
FREQUENCY MHz	MAGNITUDE dB	ANGLE DEG	MAGNITUDE dB	ANGLE DEG
1	12.5	178.1	.010	0.1
1.5	12.5	177.8	.020	0.0
2.5	12.4	176.9	.019	-0.2
4	12.4	176.4	.024	-0.5
6	12.4	174.9	.025	-0.8
10	12.3	171.3	.018	-1.5
15	12.1	167.0	.001	-2.2
25	11.8	158.3	-.001	-3.7
40	11.3	146.3	-.018	-5.9
60	10.4	132.2	-.070	-8.7
100	8.1	111.0	-.121	-14.0

MEASURED S-PARAMETERS

SINGLE STAGE COMMON EMITTER AMPLIFIER

(output bias current = .4 ma)

FREQUENCY MHz	S_{11} MAGNITUDE dB	S_{11} ANGLE DEG	S_{12} MAGNITUDE dB	S_{12} ANGLE DEG
2.5	-2.20	-1.1	-72.6	9.8
4	-2.21	-1.7	-71.6	28.0
6	-2.23	-2.7	-70.1	39.5
10	-2.25	-4.4	-67.3	56.0
15	-2.33	-6.6	-64.5	58.5
25	-2.54	-10.6	-61.0	61.9
40	-2.95	-15.5	-57.5	59.2
60	-3.55	-20.5	-55.1	54.1
100	-4.54	-26.7	-52.8	48.3

FREQUENCY MHz	S_{21} MAGNITUDE dB	S_{21} ANGLE DEG	S_{22} MAGNITUDE dB	S_{22} ANGLE DEG
2.5	13.2	176.7	-.01	-0.2
4	13.2	175.1	.00	-0.4
6	13.2	173.3	-.01	-0.8
10	13.1	168.7	-.02	-1.5
15	12.9	163.1	-.01	-2.5
25	12.4	152.2	-.04	-4.1
40	11.5	137.8	-.08	-6.2
60	10.1	121.9	-.14	-8.9
100	7.1	99.8	-.20	-14.3

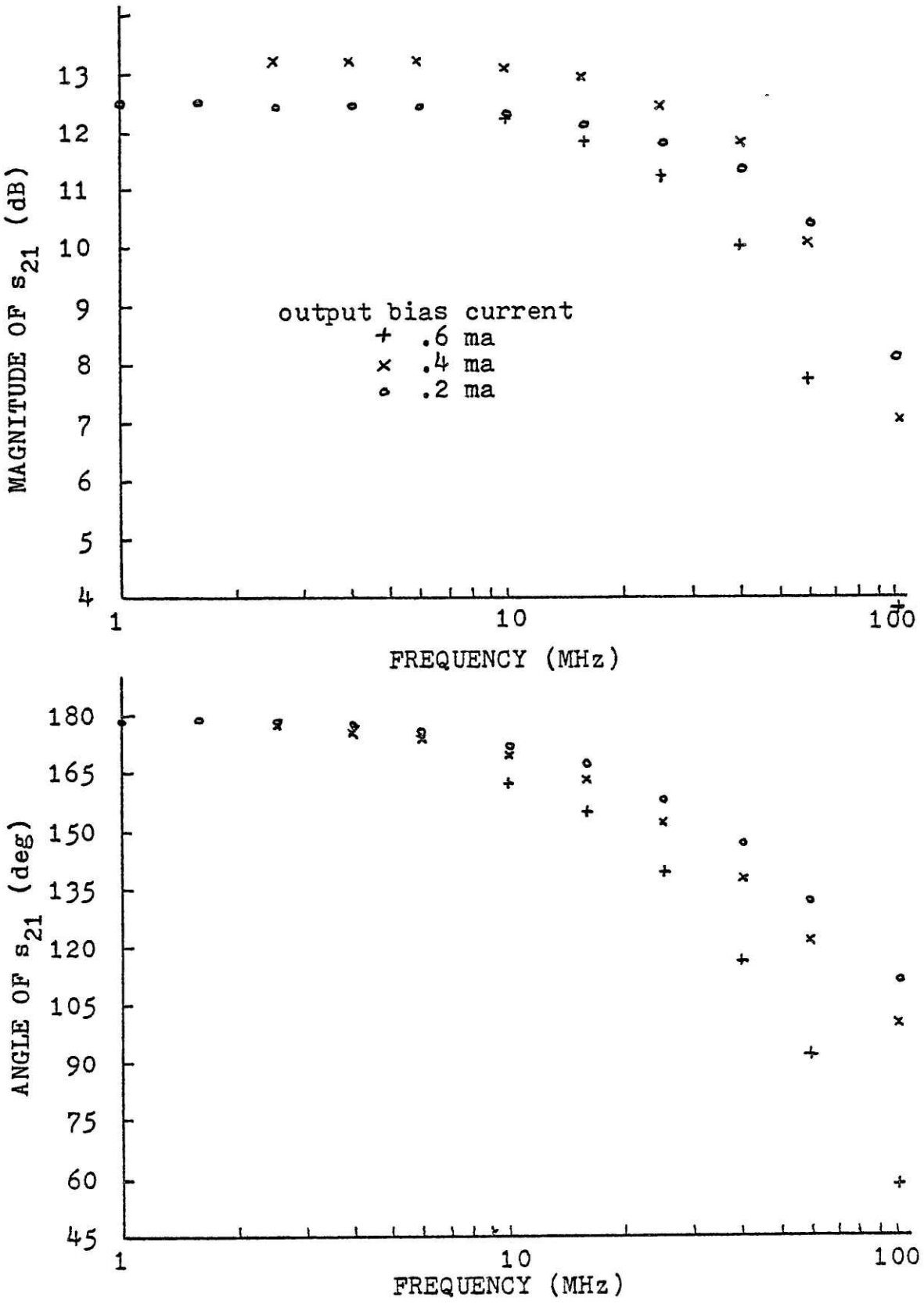
MEASURED S-PARAMETERS

SINGLE STAGE COMMON EMITTER AMPLIFIER

(output bias current = .6 ma)

FREQUENCY MHz	S_{11} MAGNITUDE dB	S_{11} ANGLE DEG	S_{12} MAGNITUDE dB	S_{12} ANGLE DEG
10	-3.52	-8.5	-61.4	33.2
15	-3.62	-11.6	-59.4	37.2
25	-3.88	-18.4	-56.0	39.1
40	-4.50	-27.8	-53.0	29.8
60	-5.33	-37.8	-51.4	17.0
100	-6.56	-55.1	-50.1	-1.7

FREQUENCY MHz	S_{21} MAGNITUDE dB	S_{21} ANGLE DEG	S_{22} MAGNITUDE dB	S_{22} ANGLE DEG
10	12.2	162.0	-0.66	-5.2
15	11.8	154.3	-0.80	-6.8
25	11.2	139.0	-0.79	-10.4
40	10.0	116.0	-0.65	-17.8
60	7.7	91.9	-0.82	-27.4
100	3.8	58.1	-1.15	-46.0



MEASURED RESPONSE
SINGLE STAGE COMMON EMITTER AMPLIFIER

MEASURED S-PARAMETERS

EIGHT STAGE COMMON EMITTER AMPLIFIER

(output bias current = .5 ma)

	S_{11}		S_{12}	
FREQUENCY MHz	MAGNITUDE dB	ANGLE DEG	MAGNITUDE dB	ANGLE DEG
10	-6.95	-17.9	-54.3	77.4
15	-6.95	-25.8	-51.4	74.2
25	-7.09	-41.7	-47.1	67.8
40	-7.97	-68.1	-43.8	58.9
60	-8.79	-95.9	-41.8	50.7
100	-9.31	-129.4	-39.7	43.1

	S_{21}		S_{22}	
FREQUENCY MHz	MAGNITUDE dB	ANGLE DEG	MAGNITUDE dB	ANGLE DEG
10	17.7	160.2	-0.06	-4.2
15	17.7	156.6	-0.15	-6.3
25	16.4	148.6	-0.35	-10.0
40	17.3	133.8	-0.71	-14.6
60	18.7	118.4	-1.13	-18.8
100	17.6	97.0	-1.65	-25.8

MEASURED S-PARAMETERS

EIGHT STAGE COMMON EMITTER AMPLIFIER

(output bias current = 1 ma)

FREQUENCY MHz	S_{11} MAGNITUDE dB	S_{11} ANGLE DEG	S_{12} MAGNITUDE dB	S_{12} ANGLE DEG
1	-12.0	-2.8	-67.4	70.2
1.5	-12.0	-4.5	-66.3	60.9
2.5	-12.0	-7.8	-64.9	68.8
4	-12.0	-12.9	-61.9	70.9
6	-11.9	-19.3	-58.6	73.7
10	-11.8	-31.5	-54.5	73.3
15	-11.4	-45.3	-51.2	71.1
25	-10.9	-70.3	-47.5	64.2
40	-10.4	-100.4	-44.6	55.9
60	-9.8	-125.2	-42.8	49.2
100	-9.1	-150.2	-40.9	44.5
150	-8.6	-169.6	-89.3	44.1
250	-8.0	164.9	-36.7	44.8

FREQUENCY MHz	S_{21} MAGNITUDE dB	S_{21} ANGLE DEG	S_{22} MAGNITUDE dB	S_{22} ANGLE DEG
1	19.6	169.4	-0.11	-0.1
1.5	19.3	168.1	-0.10	-0.4
2.5	19.0	162.8	-0.09	-1.1
4	18.8	158.7	-0.09	-1.8
6	18.6	157.3	-0.09	-2.9
10	17.8	156.2	-0.15	-4.9
15	16.8	152.4	-0.26	-7.3
25	16.2	142.2	-0.55	-11.5
40	17.3	126.4	-1.02	-15.9
60	18.8	110.8	-1.51	-19.8
100	17.5	90.2	-1.98	-26.3
150	15.1	72.5	-2.25	-34.6
250	10.4	45.9	-2.51	-53.1

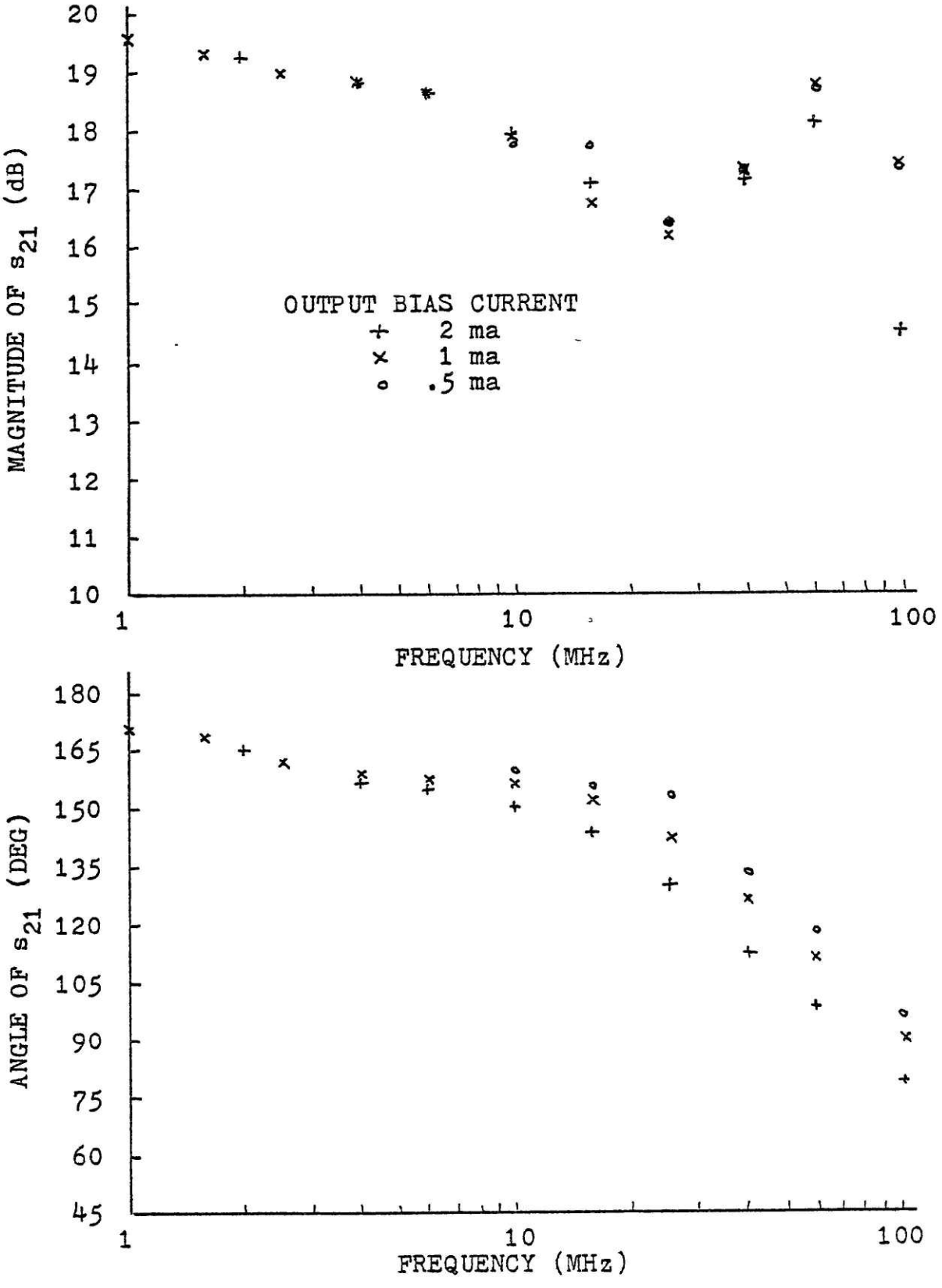
MEASURED S-PARAMETERS

EIGHT STAGE COMMON EMITTER AMPLIFIER

(output bias current = 2 ma)

FREQUENCY MHz	S_{11} MAGNITUDE dB	S_{11} ANGLE DEG	S_{12} MAGNITUDE dB	S_{12} ANGLE DEG
2	-25.2	-34.1	-57.5	25.5
4	-22.9	-56.5	-55.4	40.4
6	-20.8	-72.0	-53.1	48.9
10	-17.4	-91.6	-49.5	54.0
15	-14.9	-105.0	-47.0	53.3
25	-11.8	-125.0	-43.6	48.3
40	-9.8	-142.8	-41.4	41.6
60	-8.7	-155.0	-40.1	37.4
100	-7.8	-171.0	-38.6	36.4

FREQUENCY MHz	S_{21} MAGNITUDE dB	S_{21} ANGLE DEG	S_{22} MAGNITUDE dB	S_{22} ANGLE DEG
2	19.2	164.5	-0.82	-1.1
4	18.8	156.9	-0.79	-3.1
6	18.6	154.3	-0.83	-5.2
10	17.9	150.6	-1.04	-9.2
15	17.1	143.9	-1.36	-12.9
25	16.4	130.4	-2.15	-19.2
40	17.1	113.1	-3.16	-24.4
60	18.1	99.0	-4.01	-27.9
100	14.5	79.0	-4.83	-33.8



MEASURED RESPONSE
EIGHT STAGE COMMON EMITTER AMPLIFIER

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