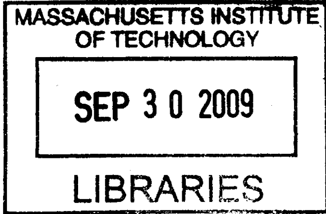
High-Speed Modulation of Resonant CMOS Photonic Modulators in Deep-Submicron Bulk-CMOS



by

Benjamin Moss

Submitted to the Department of Electrical Engineering and Computer Science

in partial fulfillment of the requirements for the degree of

Master of Science in Computer Science and Engineering

at the

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Abstract

Processor manufacturers have turned to parallelism to continue to improve processor performance, and the bandwidth demands of these systems have risen. Silicon photonics can lower the energy-per-bit of core-to-core and core-to-memory interconnects to help alleviate bandwidth bottlenecks. In this thesis, methods of controlling the amount of charge entering the PiN-diode structure of a photonic ring modulator are investigated to achieve high energy-efficiency in a constrained monolithic process. A digital modulator driver circuit is designed, simulated, fabricated and partially tested. This circuit uses a push-pull topology with preemphasis to reduce the energy per bit and to prevent the ring's optical passband from shifting to the next optical channel. A flexible driver test circuit for in-situ device characterization has been developed with a device-to-circuit modeling framework. There are many tradeoffs that must be analyzed from the system, circuit, and device levels.

Thesis Supervisor: Vladimir Stojanović
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Chapter 1

Introduction

Existing electrical high-speed chip-to-chip interconnects will be unable to cope with the increasing communication demands of systems with multi-core architectes. Circuit designers are looking to new technologies to help alleviate this developing bottleneck. Given the power constrained and cost-sensitive nature of the problem, only technologies that offer high bandwidth density (or, equivalently, low area), good energy efficiency, and compatibility with existing mainstream manufacturing methods such as bulk-complimentary-metal-oxide-semiconductor (bulk-CMOS) and thin-silicon-on-insulator (thin-SOI) will be feasible contenders to strictly electrical designs [2]. This problem spans many layers, and new technologies must be evaluated at the system, circuit and device levels. One promising new technology is integrated silicon photonics, which can take advantage of dense wavelength-division multiplexing (DWDM) to offer good bandwidth density and high energy efficiency. To motivate our efforts in building monolithic fully-integrated photonics, this thesis will simplify a proposed monolithically integrated silicon-photonic multi-core system into an example optical high-speed link circuit which can be analyzed in detail. The focus will be on the simulation, design, and testing of one of the most critical system components, the electrical-to-optical ring modulator and its driver circuit. Traditionally this device has been a speed, area, and power limiter. We propose a driver circuit that uses an all-digital push-pull topology with pre-emphasis to inject charge into the modulator device's P-I-N diode structure. The use of pre-emphasis increases the operating speed

of the modulator device while lowering power consumption. A flexible driver circuit is necessary because some critical device parameters, such as the diode's carrier lifetime, are poorly controlled by the CMOS foundry and are unknown at design time.

Two test platforms for evaluating and characterizing monolithically integrated photonics have been taped out in conventional Texas Instruments bulk-CMOS processes and preliminary measurements have been made. The purpose of the first EOS1 test platform is primarily to characterize optical properties of the photonic devices. The EOS1 chip also included a first generation modulator driver circuit. The second EOS2 platform aims to demonstrate a full electrical-to-optical-to-electrical link circuit in bulk-CMOS. The EOS2 chip includes a more flexible modulator driver to account for unknown device parameters, as well as more sophisticated electrical infrastructure to aid in experimental testing. A motivation for this thesis is the understanding of the required interplay between circuit design and device modeling for these test platforms.

Chapter 2

Background

2.1 Motivation

Over the past several years there has been a slowdown in uniprocessor performance due to power density constraints, diminishing returns of instruction-level parallelism, wire delays, and direct random access memory (DRAM) access latency [16]. This slowdown has prompted all major processor manufacturers to embrace parallelism and shift to multicore architectures, where multiple simpler cores exploit thread and data level parallelism [9]. The first dual-core processor, IBM's POWER4, arrived in December 2001 [14]. Moore's Law quickly took effect on the number of processor cores, scaling further with each progressive technology node. Dozens or even hundreds of cores (in the case of the picoChip digital signal processor family [10]) are now being designed on a single die to improve very-large-scale integrated (VLSI) system performance. The core count is expected to continually increase to maintain a steady performance improvement, leading us in the coming decade to the *manycore era* shown in Figure 2-1. A corresponding increase in main memory bandwidth is necessary if the increased core count is to result in improved application performance [2].

Power density, wire delays and DRAM access latency are not scaling with Moore's Law. Poor scaling of electrical interconnects in terms of energy-efficiency and data rate limits the throughput scaling of the whole system due to on-chip power and pin-

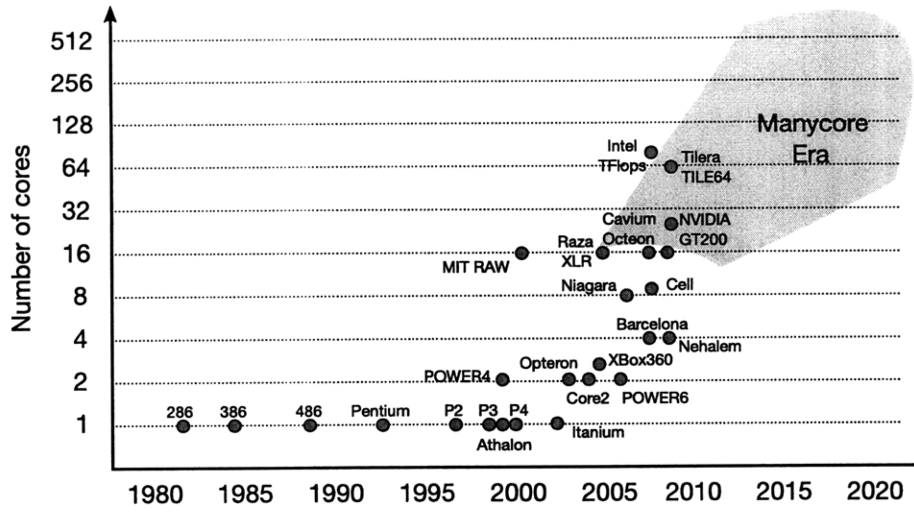


Figure 2-1: Scaling of manycore systems [4]

density limitations. Projected future electrical DRAM interfaces such as XDR [9] and FB-DIMM [19] are not expected to meet the huge bandwidth demands of manycore systems with reasonable power consumption and packaging cost. Two bottlenecks will occur in these systems, shown in Figure 2-2; one in the on-chip and one in the off-chip interconnect network. The on-chip network facilitates communication from core to core and also between cores and the primary on-chip L2 cache. The off-chip network handles communication between the on-chip cache and off-chip DRAM. Because the bandwidth provided by future electrical interconnects will be insufficient for these multi-core systems, alternate technologies such as silicon photonics must be considered to alleviate the bottlenecks.

2.2 A New Technology: Silicon Photonics

New technologies at various levels of maturity are rising to the task of meeting this *manycore bandwidth challenge.* Basic requirements for a feasible contender to electronic interconnects include high bandwidth density (or, equivalently, low area and packaging), good energy efficiency, and compatibility with existing processor design processes, i.e. bulk-CMOS and thin-SOI. Using silicon for integrated optical intercon-

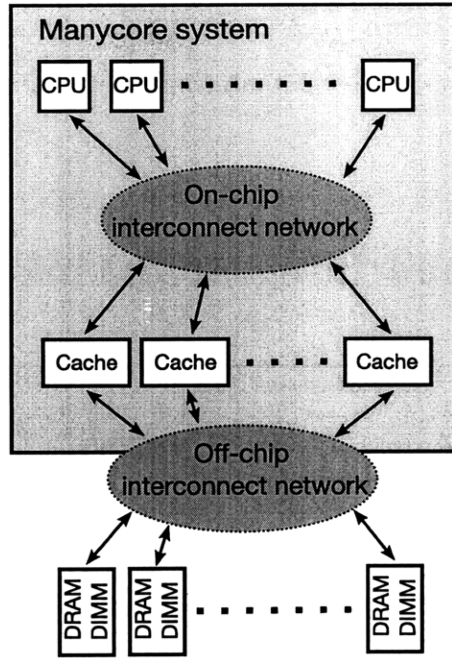


Figure 2-2: Interconnect bottlenecks in a manycore system

nects is an idea that has existed for decades and has been suggested since the 1970s [18]. The high propagation losses due to scattering, low electrooptic coefficient, low light-emission efficiency and high coupling losses prevented this technology from being adopted until the last few years, as deep-submicron fabrication techniques became advanced enough to create photonic devices [6].

Silicon photonics shows promise in reducing the power per bit for long wires, which can help reduce the bottleneck. Previous demonstrations of integrated silicon photonics [1][7] have relied on specialized thick buried oxide SOI processes which are not suitable for processor design due to the thermal isolation properties of thick oxide and the effect on transistor electrostatics. Moreover, the mainstream VLSI technology is bulk-CMOS which does not have any buried oxide layers. Adding extensive process customizations to mainstream processes is prohibitively expensive and raises the barrier for adoption, especially considering that the technology is still in developmental stages which would make it a riskier investment. Our research group has participated in the development of a general method of enabling silicon photonics in bulk-CMOS and thin-SOI without changes at the process foundry, which

is a significant step forward for the technology [8]. In addition, monolithic integration also reduces the area and energy costs of interfacing electrical and optical components [2].

2.3 A Conceptual Integrated Link

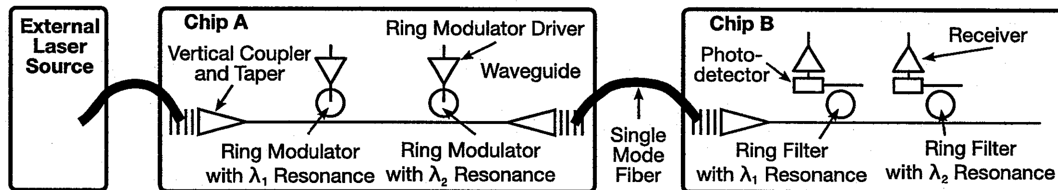


Figure 2-3: A conceptual integrated link [2]

Figure 2-3 illustrates the concept of a fully integrated silicon photonics system, where a multi-core processor uses a simple DWDM link for both on-chip (core-to-core) and chip-to-chip (core-to-memory) communication. Due to the indirect silicon bandgap, there are no known high-efficiency laser sources in Si, so unmodulated light must come from an off-chip laser source [2]. In this example, two continuous wavelengths of light (λ_1,λ_2) come from an off-chip laser and are carried by a single-mode optical fiber. The fiber arrives perpendicular to the surface of chip A, where a vertical coupler grating tapers the light into an on-chip photonic waveguide. This photonic waveguide is designed in the poly-silicon layer (which is traditionally used for transistor gates) on top of the shallow trench isolation (STI). The photonic waveguide carries the unmodulated light past a series of resonant ring modulators [5], which modulate the intensity of the light at the resonant wavelength. Modulated light continues through the waveguide, exits chip A through a vertical coupler grating into another optical fiber, and is then coupled via a vertical coupler grating into an on-chip waveguide on chip B. On chip B, each of the two receivers uses a tuned resonant ring filter to "drop" the corresponding wavelength from the waveguide into a local photodetector. Although not shown in Figure 1, information can be simultaneously sent in the reverse direction using different wavelengths (λ_3,λ_4) coupled into the same

waveguide on chip B and received by chip A.

Comparing Figure 2-2 to Figure 2-3 also reveals another key advantage of this architecture; two separate interconnect networks have now been unified into a single network, further lowering the overhead necessary. This conceptual diagram also shows how DWDM drastically increases the energy efficiency of the system by combining several wavelengths onto one waveguide without increasing the area overhead.

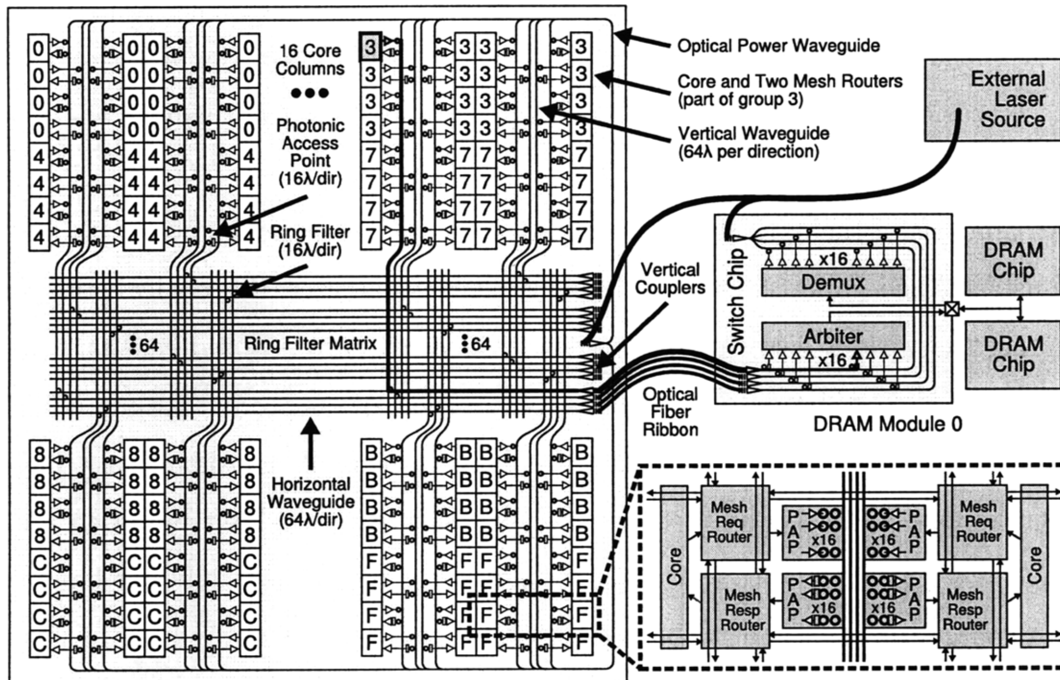


Figure 2-4: A 256-Core integrated photonic system [2]

Figure 2-4 diagrams a more sophisticated 256-core integrated photonic system based on the conceptual DWDM link presented earlier. DWDM is heavily leveraged for high density; now a single waveguide will be carrying approximately 64 wavelengths per direction for a total of 128 λ, achieving over 100x improvement in bandwidth density compared to an off-chip electrical link and over 10x compared to an on-chip electrical link. From a system architecture standpoint, the cores have been combined into groups of 16, with each core and its corresponding two mesh routers displaying a label indicating its group. The datapath between a single Group 3 core and an off-chip DRAM module is emphasized.

64 unmodulated wavelengths of light from an external laser source couple onto the chip. After the light passes through a splitter, the ring modulator on the emphasized core modulates the light on a particular λ. This modulated light continues down the chip until it meets the ring filter matrix. A ring filter drops the λ onto a perpendicular waveguide, and light exits the chip onto an optical fiber ribbon, where it enters the off-chip DRAM module. It is then filtered into a photo diode and the data reaches the electronic arbiter module. The return path of the data is identical. The total area overhead of the photonic structures in this design is 7% of the active chip area, which is feasible and tolerable. There are approximately 200 waveguides and 40,000 rings, with a total throughput of 40 Tb/s.

An analysis of the optical power budget for this full system, shown in Table A.1, demonstrates the importance of optimizing the designs of critical optical structures. Summing the various losses along the datapath in the unoptimized case and taking into account the estimated receiver sensitivity yields an outrageous estimated external laser power of 3.3 kW. Optimizing the designs to improve crossing loss, on-chip waveguide loss, and drop loss reduces the necessary external laser power to a more manageable 6.38 W. Notice that the modulator insertion loss, while not one of the largest sources of loss, is not to be neglected and also must be optimized. In this link budget, the modulator carries the biggest footprint and must be carefully optimized.

2.4 Silicon Photonics Area and Energy Advantage

To system designers developing the next generation of technology, a fair comparison is necessary to determine if the apparent advantages of an optical system will outshine the predicted performance of upcoming electrical links. Integrated silicon photonics is still years away from becoming mainstream, so comparing a projected photonic system to the current state-of-the-art electrical case would be unfair. For this reason the full system from Figure 2-4 is compared to projected electrical links in the 22 nm CMOS process node, which is still several years away.

Our analysis, shown in Table 2.1, suggests that the total energy overhead for the

Metric	**Energy (pJ/b)**	**Bandwidth Density (Gb/s/μm)**
Global on-chip photonic link	0.25	160-320
Global on-chip optimally repeated electrical link	1	5
Off-chip photonic link (50 μm coupler pitch)	0.25	13-26
Off-chip electrical SERDES (100 μm pitch)	5	0.1
On-chip/off-chip seamless photonic link	0.25	

Table 2.1: Area and Energy Comparison of Electrical and Optical Systems

various electrical back-end components of a global on-chip photonic link will be less than 250 fJ/b, which is fivefold more efficient than a global on-chip optimally repeated electrical link. This electrical backend is shown in Figure 2-5. To achieve the target energy overhead of 250 fJ/b, an optically-distributed clock is necessary to avoid the energy cost of a phase-locked loop (PLL). This optical energy overhead is also is 1-2 orders of magnitude less than state-of-the-art photonic devices [7] (not displayed in the table) because the monolithically integrated approach lowers the capacitance of photonic structures.

The anticipated bandwidth density of photonics is 32-64x higher for the on-chip case. Similar gains are seen for the off-chip case, with photonics projecting a 25x energy improvement and a 130-260x improvement in bandwidth density. Furthermore, as shown in Figure 2-3, the on-chip and off-chip photonic links can be unified with a single energy cost, only further justifying the development of this technology. It is important to note that external laser power is not factored into this energy estimate because modern processors are *on-chip* power-density limited, and the laser will be powered from an external supply.

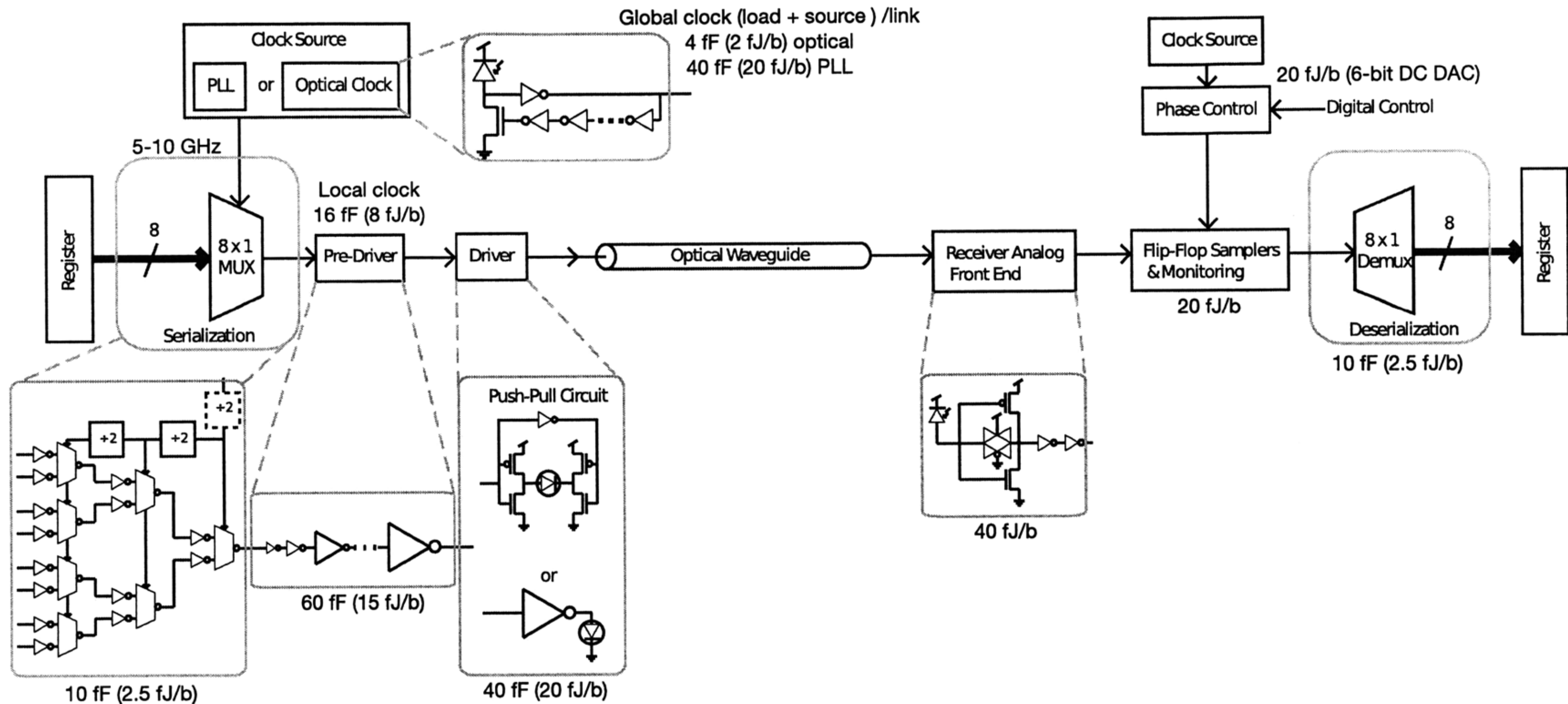


Figure 2-5: Electrical backend of a photonic link

A brief analysis of the latency of the full photonic system (shown in Table A.2) indicates that the latency of electrical and photonic systems is comparable.

The result of these analyses suggests that an integrated photonic system will need to be optimized from multiple layers (system, circuit and device) to become competitive with electrical links. The modulator is one of the most fundamental parts of this system and is critical both from an energy effeciency and bandwidth perspective, which is the motivation for this thesis.

Chapter 3

The Ring Modulator

The modulator is a fundamental building block of any electrical-to-optical system. In contrast to passive photonic devices such as vertical couplers, splitters, and ring filters, the modulator is an active device which can electrically turn on and off the light flowing through it at a particular wavelength.

The forward-biased charge-injection ring modulator is a tunable resonant ring filter. The optical frequency response of this filter follows a Lorentzian distribution, shown in Figure 3-1 [12]. Light is modulated by shifting the stopband of the resonant filter in and out of the optical channel. As the stopband shifts by some Δf (shown as 20 GHz in the figure), the transmissivity of the filter rises from T_0 to T. The *extinction ratio* of the modulator is defined as $h = T/T_0$ (or, in decibels, $h_{dB} = T_{dB} - T_{0dB}$). The stopband is shifted by changing the refractive index of the ring, which can be accomplished by two mechanisms.

The pioneering work of Soref [13] showed that the free-carrier plasma dispersion effect can change the refractive index of silicon. This effect was originally used to provide a phase shift in branches of Mach-Zehnder (MZ) modulators [7] and more recently to change the resonance of ring modulators [20] such as ours [8]. In order to inject large amounts of charge into the ring's waveguide, a P-I-N diode structure is created with the intrinsic polysilicon waveguide acting as the I-region.

In addition to charge concentration, ring resonance is also sensitive to temperature. Although far too slow for data transmissions, this effect is useful to adjust the ring's

resonance to account for process variation. We fabricate polysilicon heaters near the rings to both heat the rings and serve as temperature sensors. Compact analog-to-digital (ADCs) and digital-to-analog converters (DACs) can be used to digitize the temperature information.[1]

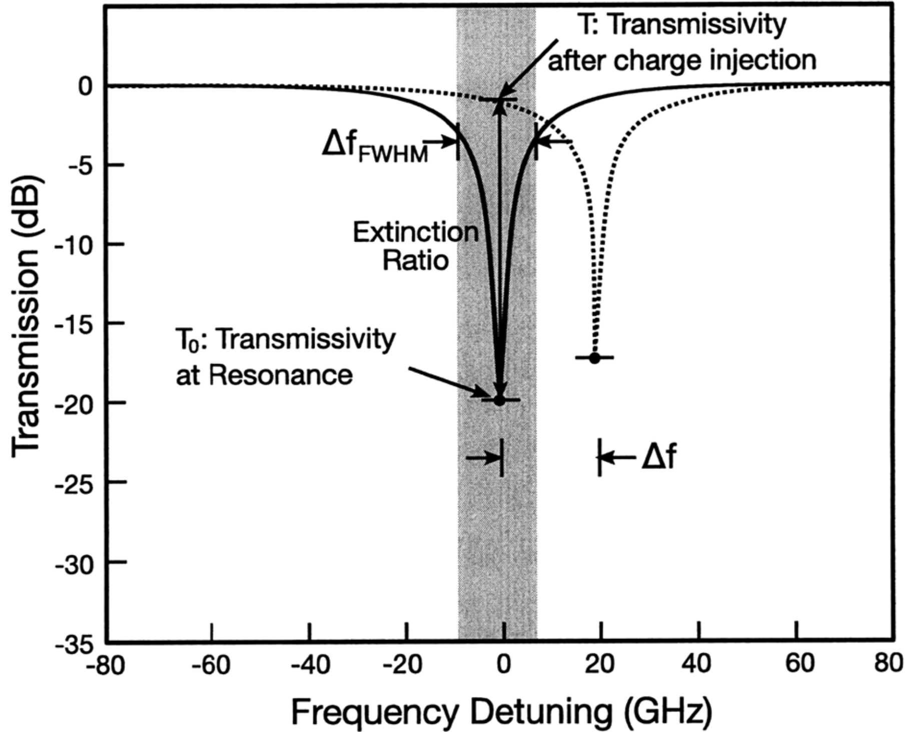


Figure 3-1: Ring modulator Lorentzian frequency response.

3.1 Ring Modulator Geometry

A top-view diagram of the ring modulator is shown in Figure 3-2. The modulator is fabricated in the polysilicon layer usually intended for transistor gates. The waveguide poly is doped as little as possible and unsilicided to preserve its optical properties. Unmodulated light at the target optical channel λ_0 travels down the waveguide until it reaches the In port of the modulator. Because λ_0 is at the ring's resonant wavelength, light couples into the ring and travels counter-clockwise until it exits the Drop port.

[1] We have fabricated a novel energy-efficient charge-redistribution successive approximation ADC in a 90 nm process which would be suitable for this purpose.

The other optical channels pass to the Through port unaffected. If the modulator has a perfect extinction ratio and is properly tuned, no light at λ_0 continues down the Through port. A certain amount of time is necessary for the resonance to build up inside the ring, but the ring's optical response is fast in comparison to its electrical response and can be neglected.

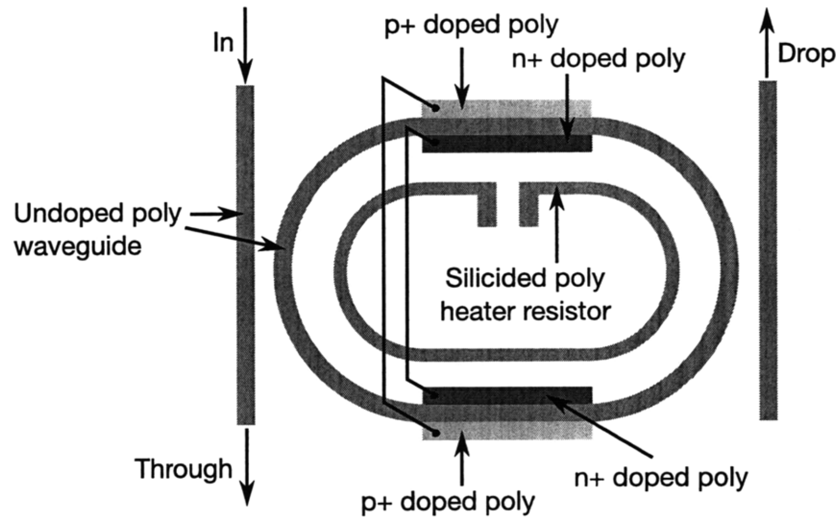


Figure 3-2: Ring modulator diagram (not to scale).

Due to the limitations of fabricating curved structures on a Manhattan grid, the ring is elongated into a racetrack shape so that the P-I-N diode structure can occupy a straight section of the waveguide [8]. Figure 3-3 also shows the geometry of the P-I-N structure in finer detail. The intrinsic poly waveguide has connections on one side to thin p+ unsilicided poly fingers and on the other side to n+ fingers. Farther from the waveguide, the finger tapers out to a silicided section with tungsten contacts to the first metal layer.

There are several tradeoffs associated with the finger design. The fingers disrupt the optical mode and cause loss, lowering the ring's quality factor $\mathbb{Q}$ and making it more difficult to achieve good modulation depth. However, the fingers have high resistance, and too few fingers will cause the series resistance of the diode to be high, making charge injection difficult. A similar tradeoff exists with the choice of how far to place the diffusion region from the waveguide. Having the highly-doped region

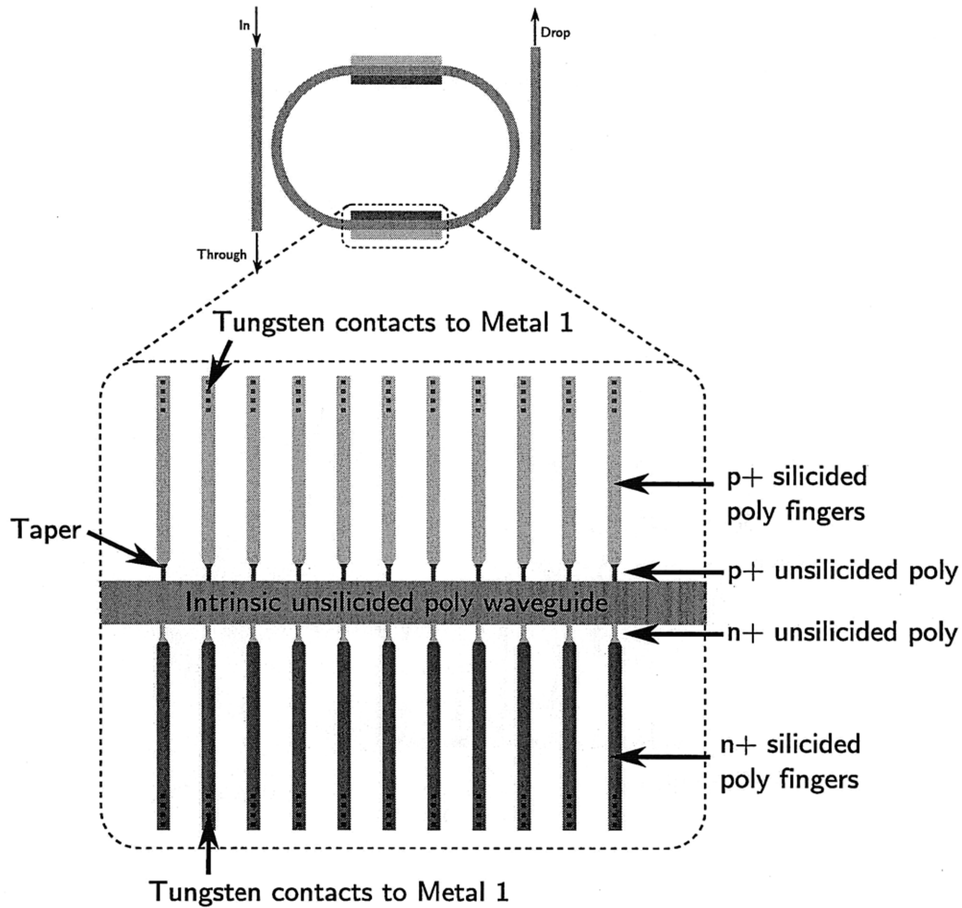


Figure 3-3: P-I-N finger structure.

close to the waveguide increases loss but makes it easier to inject charge by having a lower diode body length. The finger spacing is also a critical parameter which must be carefully chosen by the device designers.

3.2 Optical Modulation by Charge Injection

From a circuit designer's perspective, the ring modulator is a P-I-N diode structure which must have charge dynamically injected into it. Modulator models in both the circuit and device domain are necessary to predict and verify the operation of the circuit. A link between the electrical and optical domain is however necessary to design and simulate a working circuit to modulate light. This section will analytically

demonstrate that link.

The ultimate goal is to create a working electrical-to-optical-to-electrical link. The photodiode and receiver sensitivity will determine the minimum extinction ratio that can be tolerated. The goal of this section is to describe an analytical method to determine the amount of charge injection necessary to produce a given optical extinction ratio. This is an important tool for circuit designers and is used in development of the modulator driver circuit.

3.2.1 Ring Modulator Dimensions

Some racetrack dimensions must first be defined, shown in Figure 3-4. The length of a single junction in the direction of optical propagation is L_j. There are two such junctions in the ring. The ring's radius in the curved section is r and its total circumference is $L_{tot} = 2L_j + 2\pi r$. The waveguide's height is H and its width is W. The volume of the waveguide diode junction is $V_j = 2 \cdot L_j \cdot W \cdot H$.

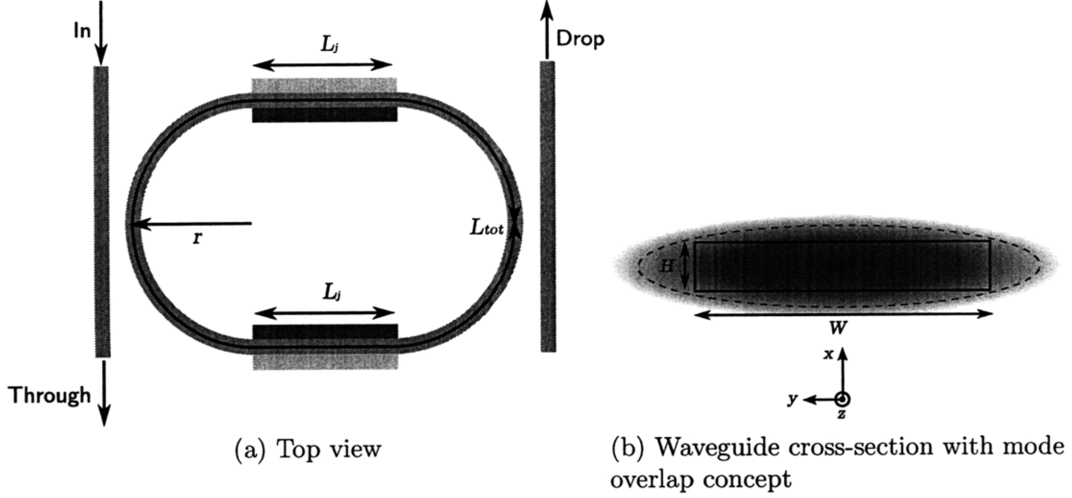
Some terminology is necessary to clarify a sticking point of confusion regarding the diode dimensions. The junction length L_j (a parameter important in the optical domain) is equivalent to the diode width W_d (a parameter important in the circuit and device domains). Similarly, the waveguide width W is equivalent to the diode length L_d. This terminology preserves the intuition that a wider diode will draw more current at a given voltage.

3.2.2 Free Spectral Range

Light traveling through the ring at its resonant wavelength λ_0 (prior to charge injection) must travel an integer number of wavelengths m in one round trip L_{tot} [6], given by

$$\frac{L_{tot}}{\lambda_0} = \frac{k_0 \cdot L_{tot}}{2\pi} = m \tag{3.1}$$

The wavenumber of the light is $k_0 = \frac{2\pi}{\lambda_0} = \frac{\omega_0}{c_0}$. The frequency spacing between the ring's resonances, the free spectral range (FSR), is determined by the frequency



(a) Top view

(b) Waveguide cross-section with mode overlap concept

Figure 3-4: Ring modulator dimensions (heater ommitted)

change required to shift the integer number of wavelengths by one.

$$\frac{k_{FSR} \cdot L_{tot}}{2\pi} = 1 \tag{3.2}$$

$$\frac{\omega_{FSR} \cdot L_{tot}}{c_0 \cdot 2\pi} = 1 \tag{3.3}$$

$$\frac{FSR \cdot L_{tot}}{c_0} = 1 \tag{3.4}$$

$$FSR = \frac{c_0}{L_{tot}} = 1 \tag{3.5}$$

$$FSR = \frac{c}{L_{tot} \cdot n_g} \tag{3.6}$$

The speed of light in free space is c and the speed of light within the waveguide is $c_0 = \frac{c}{n_g}$, n_g being the group index of the ring. For 1220 nm, $n_g = 3.3$.

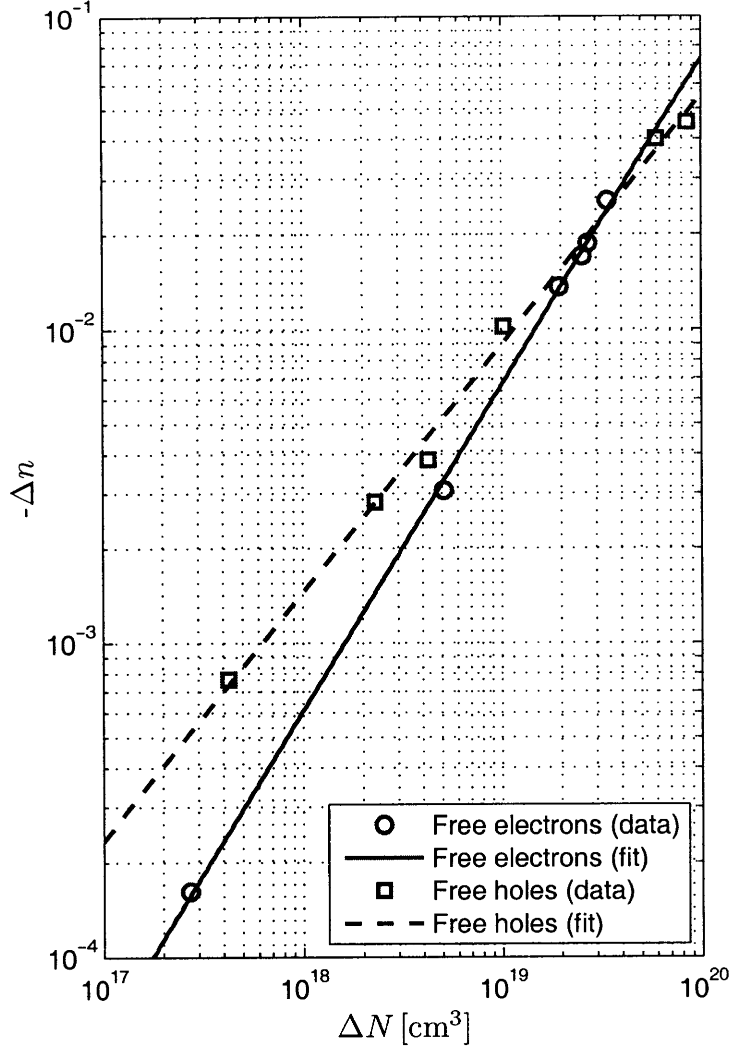


Figure 3-5: Silicon free carrier index change at $\lambda = 1220\,\text{nm}$[13]

3.2.3 Free Carrier Refractive Index Change

As free electrons and holes are injected into the two I-regions, the index of refraction (Δn) in those regions will decrease. The index change is sensitive to both free electron concentration ΔN_e and free hole concentration ΔN_h.

$$\Delta n = \Delta n_e + \Delta n_h = n_{fe}\Delta N_e + n_{fh}(\Delta N_h)^{0.8} \tag{3.7}$$

Experimental data by Soref [13] has empirically determined the values of n_{fe} and n_{fh} at $\lambda = 1300\,\text{nm}$. The ring modulators we are using are designed for $\lambda = 1220\,\text{nm}$,

so Soref's data must be extrapolated. The theoretical model for refraction due to free carriers is shown in Equation 3.8 and shows a dependence on λ^2, where e is the electronic charge, ϵ_0 is the permittivity of free space, n is the refractive index of unperturbed silicon, $m_{ce}*$ is the conductivity effective mass of electrons, and $m_{ch}*$ is the conductivity effective mass of holes [13].

$$\Delta n = -(e^2\lambda^2/8\pi^2c^2\epsilon_0 n)[\Delta N_e/m_{ce}* + \Delta N_h/m_{ch}*] \tag{3.8}$$

The λ^2 dependence is used to adjust the $\lambda = 1300\,\mathrm{nm}$ n_{fe} and n_{fh} coefficients to be appropriate for $\lambda = 1220\,\mathrm{nm}$. The data from Figure 10 in [13] was transcribed, and each value of $-\Delta n$ was multiplied by $(1220\,\mathrm{nm})^2/(1300\,\mathrm{nm})^2$. A linear regression algorithm was used to find the new values of n_{fe} and n_{fh} at $\lambda = 1220\,\mathrm{nm}$, shown in Figure 3-5[2]. As Soref mentions, Equation 3.8 is too simplistic to take into account the measured $(\Delta N_h)^{0.8}$ dependence in Equation 3.7, and there is also a slight exponential dependence on N_e as well which is neglected, so there is a degree of inaccuracy in the result. We use the experimental model of Equation 3.7 with the values of n_{fe} and n_{fh} in Equation 3.9 which are valid for $\lambda = 1220\,\mathrm{nm}$ at injection levels of $\Delta N \approx 10^{19}\,\mathrm{cm}^3$.

$$n_{fe} = 4.8 \times 10^{-22}\,\mathrm{cm}^{-3}, \quad n_{fh} = 4.9 \times 10^{-18}\,\mathrm{cm}^{-3} \tag{3.9}$$

The index change in the intrinsic region does not have a full effect on the optical mode due to the mode overlapping the waveguide as shown in Figure 3-4b. The charge injected in the I-region does not fully overlap with the mode, but only with a portion. A correction coefficient $\Gamma = 0.43$ determined through optical simulations by the photonic device designers is added to correct for this effect.

$$\Delta n_{eff} = \Delta n \cdot \Gamma, \qquad \Gamma = 0.43 \tag{3.10}$$

[2]This procedure was initially performed by Milos Popović.

3.2.4 Phase Shift Due to Refractive Index Change

The index change in the straight sections of the racetrack causes a phase shift in the light traveling in the ring, still at wavelength λ_0. The $\overline{E}$-field of single-mode light [15] through one straight section of the racetrack inside the I-region prior to charge injection can be described by a vector with the Cartesian coordinate system defined in Figure 3-4b and the light traveling in the $+\hat{z}$-direction.

$$\overline{E_0} = \hat{y}\underline{E_0}\sin(k_0 x)e^{-jk_0 L_j} \tag{3.11}$$

$\underline{E_0}$ is a phasor at the frequency of the light; the magnitude is unimportant because we only care about the phase of the light. The $\overline{E}$-field of single-mode light through one straight section of the racetrack *after* charge injection is $\overline{E_i}$.

$$\overline{E_i} = \hat{y}\underline{E_0}\sin(k_i x)e^{-jk_i L_j} \tag{3.12}$$

$$\overline{E_i} = \hat{y}\underline{E_0}\sin(n_{eff} k_0 x)e^{-jn_{eff} k_0 L_j} \tag{3.13}$$

The index change is seen in the term $k_i = k_0 n_{eff} = \frac{\omega_0 n_{eff}}{c_0}$. The phase change of the light $\Delta\phi'$ can be described by comparing the phase of these two cases in Equations 3.11 and 3.13 (neglecting any magnitude changes).

$$\Delta\phi' = (n_{eff} k_0 L_j) - (k_0 L_j) = \Delta n_{eff} \cdot k_0 \cdot L_j \tag{3.14}$$

The light passes two of these straight regions as it traverses the ring, each with identical charge concentrations, which doubles the phase change.

$$\Delta\phi = 2 \cdot \Delta\phi' = \Delta n_{eff} \cdot 2L_j \cdot k_0 \tag{3.15}$$

3.2.5 Resonance Shift

It is useful to know how much the resonant frequency of the ring has changed by this charge injection. Earlier it was stated that prior to charge injection, because the light was at the ring's resonant wavelength, an integer number of trips are made by the light around the waveguide as $k_0 \cdot L_{tot} = 2\pi m$. Because the ring's resonant wavelength has perturbed, this relation no longer holds for an integer number of wavelengths.

$$k_0 \cdot L_{tot} + \Delta\phi = 2\pi(m + \Delta m) \tag{3.16}$$

There *are*, however, the same m integer number of wavelengths in the ring for a slightly different wavelength of light λ_i, which is the ring's new resonant wavelength. Assume the ring has not shifted by a full free spectral range (FSR) through charge injection, but rather by a small perturbation. We can solve for the new wavelength, which will initially be represented by the perturbed wavenumber $k_0 + \Delta k$.

$$(k_0 + \Delta k) \cdot L_{tot} + \Delta\phi = 2\pi m \tag{3.17}$$

$$k_0 \cdot L_{tot} + \Delta k \cdot L_{tot} + \Delta\phi = 2\pi m \tag{3.18}$$

By subtracting $k_0 \cdot L_{tot} = 2\pi m$ from Equation 3.1 earlier,

$$\Delta k \cdot L_{tot} + \Delta\phi = 0 \tag{3.19}$$

This equation is not yet in a useful form to see how the ring's resonance shifts as a result of the phase change of the light. From the general form of the dispersion relation, $k = \frac{\omega n}{c}$.

$$\Delta k = \Delta(\frac{\omega n_{eff}}{c_0}) \tag{3.20}$$

By definition,

$$\Delta k = \frac{\Delta k}{\Delta \omega} \cdot \Delta \omega \tag{3.21}$$

$$\Delta k = \frac{\Delta(\omega n_{eff})}{\Delta \omega} \cdot \frac{1}{c_0} \cdot \Delta \omega \tag{3.22}$$

The group index can be written as $n_g = \frac{\Delta(\omega n_{eff})}{\Delta \omega}$.

$$\Delta k = \frac{n_g}{c_0} \cdot \Delta \omega \tag{3.23}$$

This expression is combined with Equation 3.19 and simplified.

$$\frac{n_g L_{tot}}{c} \cdot \Delta \omega + \Delta \phi = 0 \tag{3.24}$$

The expression for FSR from Equation 3.6, $FSR = c/(L_{tot} \cdot n_g)$, is used to simplify further.

$$\frac{1}{FSR} \Delta \omega = -\Delta \phi \tag{3.25}$$

$$\frac{1}{FSR} \frac{\Delta \omega}{2\pi} = -\frac{\Delta \phi}{2\pi} \tag{3.26}$$

$$\frac{\Delta f}{FSR} = -\frac{\Delta \phi}{2\pi} \tag{3.27}$$

Equation 3.27 describes how much the ring's resonant frequency will shift (Δf) based on the phase shift of the light inside of the ring ($\Delta \phi$). This is useful because it is one step closer to an analytical link between the charge in the I-region and the transmissivity of the ring in the optical channel. As mentioned earlier, the receiver sensitivity and the laser power will determine the minimum extinction ratio that can be tolerated. T_{0dB} determines the maximum extinction ratio that is theoretically possible. The transmissivity T_{dB} cannot be greater than 0 dB, so if T_{0dB} is -10 dB, for instance, the maximum possible extinction ratio would be 10 dB.

A tradeoff between optical laser power and modulator power is evident. A large

extinction ratio requires less optical laser power for a given receiver sensitivity. However, a large extinction ratio requires higher charge injection and thus higher current and power, making it electrically more expensive and slower. A lower extinction ratio is electrically cheaper but requires higher optical laser power. An extinction ratio of 3 dB is a reasonable target because this is a twofold change in optical power between a 1-bit and a 0-bit.

The Lorentzian distribution in Equation 3.28 describes the relationship between T and $\Delta\phi$. The full-width-half-max phase shift $\Delta\phi_{HWHM}$ will change the transmissivity from T_0 to $2T_0$, or 3 dB. Note from Figure 3-1 that the ring's transmissivity at its shifted resonant frequency is higher than T_0 due to the optical loss introduced by the injected carriers. This behavior decreases the extinction ratio, but it is not modeled in this analysis. The insertion and through loss is also affected with higher carrier injection.

$$T(\Delta\phi) = 1 - \frac{1 - T_0}{1 + (\frac{\Delta\phi}{\Delta\phi_{HWHM}})^2} \tag{3.28}$$

The full-width-half-max bandwidth of the ring Δf_{FWHM} (shown graphically in Figure 3-1) and full-width-half-max phase shift $\Delta\phi_{FWHM}$ are related by Equation 3.27.

$$\frac{\Delta f_{FWHM}}{FSR} = -\frac{\Delta\phi_{FWHM}}{2\pi} \tag{3.29}$$

The half-width-half-max phase shift is half of the full-width-half-max phase shift. The negative sign can be neglected because the Lorentzian distribution is symmetric.

$$2\Delta\phi_{HWHM} = \Delta\phi_{FWHM} = 2\pi \cdot \frac{\Delta f_{FWHM}}{FSR} \tag{3.30}$$

$$\Delta\phi_{HWHM} = \pi \cdot \frac{\Delta f_{FWHM}}{FSR} \tag{3.31}$$

Therefore, when the phase shift $\Delta\phi$ reaches $\Delta\phi_{HWHM}$, the optical extinction ratio will be 3 dB. The amount of charge necessary to create this phase shift is determined

by combining the expressions for $\Delta\phi$ from Equation 3.14 and $\Delta\phi_{HWHM}$ from Equation 3.31.

$$\frac{\Delta\phi}{\Delta\phi_{HWHM}} = \frac{\Delta n_{eff} \cdot 2L_j \cdot k_0}{\pi \cdot \Delta f_{FWHM}/FSR} \tag{3.32}$$

A few substitutions are necessary. From Equation 3.10, $\Delta n_{eff} = \Delta n \cdot \Gamma$; from Equation 3.6, $FSR = c/(n_g \cdot L_{tot})$, and $k_0 = 2\pi/\lambda_0$.

$$\frac{\Delta\phi}{\Delta\phi_{HWHM}} = \frac{\Delta n \cdot \Gamma \cdot 2L_j \cdot 2\pi}{\lambda_0 \cdot \pi \cdot \Delta f_{FWHM}} \cdot \frac{c}{n_g \cdot L_{tot}} \tag{3.33}$$

From Equation 3.7, $\Delta n = n_{fe}\Delta N_e + n_{fh}(\Delta N_h)^{0.8}$, and the ring's total length L_{tot} is a combination of the two straight sections and the two curved sections; $L_{tot} = 2L_j + 2\pi r$.

$$\frac{\Delta\phi}{\Delta\phi_{HWHM}} = \frac{[n_{fe}\Delta N_e + n_{fh}(\Delta N_h)^{0.8}] \cdot \Gamma \cdot 4L_j \cdot c}{\lambda_0 \cdot \Delta f_{FWHM} \cdot n_g(2L_j + 2\pi r)} \tag{3.34}$$

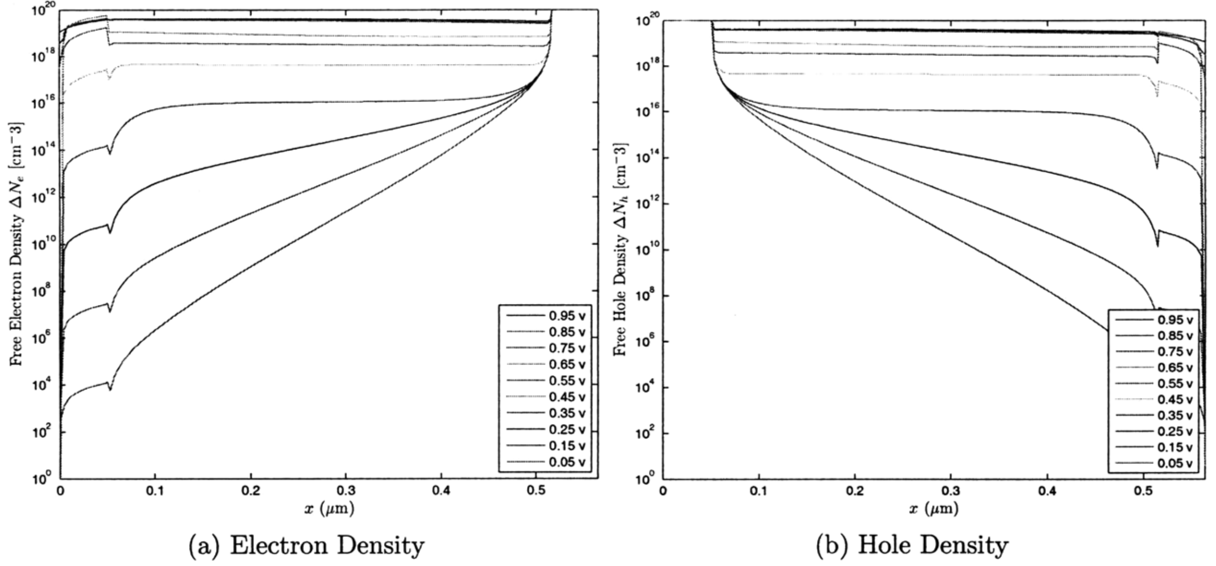
$$\gamma = \frac{\Delta\phi}{\Delta\phi_{HWHM}} \tag{3.35}$$

The ratio $\Delta\phi/\Delta\phi_{HWHM}$ is referred to as the *injection ratio* γ.

3.2.6 Uniform Carrier Injection

Figure 3-6 shows the free electron and hole concentration in the I-region cross-section with varying voltage (from Sentaurus simulations) showing the uniform charge density above $V \approx 0.4\,\mathrm{V}$. The I-region extends from $x = 0.05\,\mu\mathrm{m}$ to $x = 0.515\,\mu\mathrm{m}$. Equation 3.34 makes the assumption that the carrier injection across the I-region is uniform. A Sentaurus[3] device simulation of the cross-section of the diode is shown in Figure 3-6. In this figure, the light propagates into the page, and the anode and cathode are on the left and right sides of the graph, respectively. The result of the simulation confirms that the carrier injection is uniform across the diode's length for both ΔN_e and ΔN_h for I-region lengths of 0.5 to 2.0 μm and forward-bias voltages above 0.4

[3]Sentaurus is a software suite developed by Synopsys for device simulation.



(a) Electron Density (b) Hole Density

Figure 3-6: Free electron and hole concentration

V, well below the turn-on voltage of the diode. Also, a distinction has been made between the free electron concentration ΔN_e and the free hole concentration ΔN_h, but for forward-bias voltages above 0.4 V, these concentrations are identical, confirmed by the same Sentaurus simulation and shown in Figure B-1.

$$\Delta N = \Delta N_e = \Delta N_h \text{ for } V_D > 0.4 \text{ V} \tag{3.36}$$

ΔN now represents the free electron-hole pair concentration in the I-region.

3.2.7 Carrier Injection to Reach Half-Width-Half-Max

When $\Delta\phi = \Delta\phi_{HWHM}$ ($\gamma = 1$), the extinction ratio will be 3 dB. The charge concentration necessary to reach this extinction ratio will be defined as ΔN_0.

$$\frac{\Delta\phi}{\Delta\phi_{HWHM}} = \gamma = \frac{[n_{fe}\Delta N + n_{fh}(\Delta N)^{0.8}] \cdot \Gamma \cdot 4L_j \cdot c}{\lambda_0 \cdot \Delta f_{FWHM} \cdot n_g(2L_j + 2\pi r)} \tag{3.37}$$

$$\gamma = 1 = \frac{[n_{fe}\Delta N_0 + n_{fh}(\Delta N_0)^{0.8}] \cdot \Gamma \cdot 4L_j \cdot c}{\lambda_0 \cdot \Delta f_{FWHM} \cdot n_g(2L_j + 2\pi r)} \tag{3.38}$$

Equation 3.38 is a transcendental expression and requires an iterative numerical method to solve for ΔN_0. A simpler expression for the refractive index change Δn could be used to linearize the equation at a loss of accuracy.

3.2.8 Quality Factor

It is worth noting that Equation 3.38 can also be put in terms of the $\mathbb{Q}$ of the ring, demonstrating analytically that a higher $\mathbb{Q}$ will increase modulator performance by lowering the charge injection necessary for a given extinction ratio.

$$\mathbb{Q} = \frac{f_0}{\Delta f_{FWHM}} = \frac{c}{\lambda_0 \cdot \Delta f_{FWHM}} \tag{3.39}$$

$$\gamma = 1 = \frac{[n_{fe}\Delta N_0 + n_{fh}(\Delta N_0)^{0.8}] \cdot \Gamma \cdot 4L_j \cdot \mathbb{Q}}{n_g(2L_j + 2\pi r)} \tag{3.40}$$

3.2.9 Junction Length Tradeoff

One more discovery from Equation 3.38 is more apparent if the equation is put in terms of total carriers ΔN_{tot} rather than carrier concentration.

$$\Delta N_0 = \frac{\Delta N_{tot}}{V_j} = \frac{\Delta N_{tot}}{2L_j \cdot W \cdot H} \tag{3.41}$$

$$\gamma = 1 = \frac{[n_{fe} \cdot \frac{\Delta N_{tot}}{2L_j \cdot W \cdot H} + n_{fh} \cdot (\frac{\Delta N_{tot}}{2L_j \cdot W \cdot H})^{0.8}] \cdot \Gamma \cdot 4L_j \cdot \mathbb{Q}}{n_g(2L_j + 2\pi r)} \tag{3.42}$$

The numerator and denominator are multiplied by the total junction volume $V_j = 2L_j \cdot W \cdot H$ and the ring modulator volume $V_{tot} = (2L_j + 2\pi r) \cdot W \cdot H$ is substituted.

$$\gamma = 1 = \frac{[n_{fe} \cdot \Delta N_{tot} + n_{fh} \cdot (2L_j \cdot W \cdot H)^{0.2} \cdot (\Delta N_{tot})^{0.8}] \cdot \Gamma \cdot 2 \cdot \mathbb{Q}}{n_g \cdot V_{tot}} \tag{3.43}$$

There is a design tradeoff involved in choosing L_j for a given ring circumference.

A longer L_j will lower the series resistance of the diode, but it will also raise the junction capacitance. The significance of Equation 3.43 is that the effect of L_j on the modulation depth (for a given circumference) is weak, while it allows us to make tradeoffs at the circuit level. Notice that a larger L_j will require more current from the circuit.

3.2.10 Determining Carrier Injection for a Given Extinction Ratio

A more general form of Equation 3.38 to solve for ΔN given any extinction ratio h is a more useful tool; Equation 3.38 only solves for ΔN_0 for the specific extinction ratio of 3 dB.

$$h = T/T_0 \tag{3.44}$$

$$T = h \cdot T_0 \tag{3.45}$$

$$\tag{3.46}$$

The Lorentzian distribution describing the optical transmissivity from Equation 3.28 can be solved using the given h.

$$T(\Delta\phi) = 1 - \frac{1-T_0}{1+\gamma^2} \tag{3.47}$$

$$1 - T = \frac{1-T_0}{1+\gamma^2} \tag{3.48}$$

$$1+\gamma^2 = \frac{1-T_0}{1-T} \tag{3.49}$$

$$\gamma = \sqrt{\frac{1-T_0}{1-T} - 1} \tag{3.50}$$

$$\gamma = \sqrt{\frac{1-T_0}{1-h\cdot T_0} - 1} \tag{3.51}$$

$$\tag{3.52}$$

Equation 3.37 is combined with Equation 3.51 to find the ΔN necessary to reach this injection ratio.

$$\gamma = \sqrt{\frac{1-T_0}{1-h \cdot T_0}} - 1 = \frac{[n_{fe}\Delta N + n_{fh}(\Delta N)^{0.8}] \cdot \Gamma \cdot 4L_j \cdot c}{\lambda_0 \cdot \Delta f_{FWHM} \cdot n_g(2L_j + 2\pi r)} \tag{3.53}$$

Again, Equation 3.53 is a transcedental equation without a simple solution. The only unknown is ΔN.

3.2.11 Conclusion

This section has described an analytical method to determine the amount of charge injection necessary to produce a given optical extinction ratio. This is an important tool for circuit designers and is used in development of the modulator driver circuit.

3.3 A Ring Modulator at $\lambda = 1220$ nm

This section will use the methods of the previous section to analyze a realistic ring modulator designed for a commercial 32 nm bulk-CMOS process.

Below are some of the optical parameters and physical constants relevant to the ring modulator.

$$c = 3 \times 10^8\,\mathrm{m/s} \quad \text{(Speed of light)} \tag{3.54}$$

$$\lambda_0 = 1220\,\mathrm{nm} \quad \text{(Resonant wavelength)} \tag{3.55}$$

$$n_g = 3.3 \quad \text{(Waveguide group index)} \tag{3.56}$$

$$\Gamma = 0.42 \quad \text{(Mode overlap)} \tag{3.57}$$

$$FSR = 1.4\,\mathrm{THz} \quad \text{(Free spectral range)} \tag{3.58}$$

$$\Delta f_{FWHM} = 270\,\mathrm{GHz} \quad \text{(Ring bandwidth)} \tag{3.59}$$

$$n_{fe} = 4.8 \times 10^{-22}\,\mathrm{cm}^{-}3 \quad \text{(Refraction electron coefficient)} \tag{3.60}$$

$$n_{fh} = 4.9 \times 10^{-18}\,\mathrm{cm}^{-}3 \quad \text{(Refraction hole coefficient)} \tag{3.61}$$

$$T_0 = -10\,\text{dB} \quad \text{(Transmissivity at resonance)} \tag{3.62}$$

$$h = 3\,\text{dB} \quad \text{(Target extinction ratio)} \tag{3.63}$$

$$\gamma = 1 \quad \text{(Injection ratio for } h = 3 \text{ dB)} \tag{3.64}$$

$$\tag{3.65}$$

The ring geometry is given below using the dimensioning from Figure 3-4.

$$L_j = 6\,\mu\text{m} \quad \text{(Single junction length)} \tag{3.66}$$

$$r = 8\,\mu\text{m} \quad \text{(Bend radius)} \tag{3.67}$$

$$W = 430\,\text{nm} \quad \text{(Waveguide I-region width)} \tag{3.68}$$

$$H = 90\,\text{nm} \quad \text{(Waveguide height)} \tag{3.69}$$

$$V_j = 4.128 \times 10^{-13}\,\text{cm}^-3 \quad \text{(Diode I-region junction volume)} \tag{3.70}$$

$$L_{tot} = 62.3\,\mu\text{m} \quad \text{(Ring circumference)} \tag{3.71}$$

$$\tag{3.72}$$

The MATLAB `fzero` command was used to solve Equation 3.38 using the above parameters to find the injected charge density necessary for an extinction ratio of 3 dB.

$$\Delta N_0 = 2.1 \times 10^{18}\,\text{cm}^-3 \tag{3.73}$$

$$\Delta Q_0 = 1.9 \times 10^{-13}\,\text{C} \tag{3.74}$$

$$\tag{3.75}$$

.

These parameters were used to explore the modulator driver design space.

[3]The actual device parameters for the process are protected under a non-disclosure agreement but the given parameters are a reasonable substitute.

3.4 The P-I-N Diode

The P-I-N diode is a meeting point between the circuit and device designers. Both need accurate models of the diode to simulate and verify the behavior of the device. An accurate diode model is also necessary to analyze the numerous design tradeoffs. The development of a valid model across the optical, device, and circuit domains requires iteration between multiple simulators. The simulation design flow for developing a model for the P-I-N diode is shown in Figure 3-7.

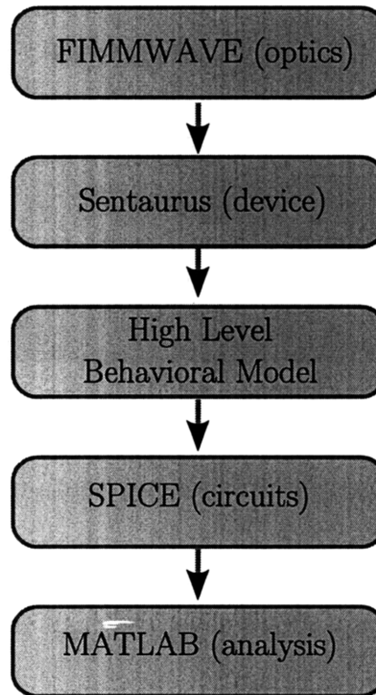


Figure 3-7: Simulation design flow.

3.4.1 Device Simulation using Sentaurus

The Sentaurus device simulator can provide a more accurate physical simulation of the P-I-N diode at the expense of poor integration with complicated circuit descriptions. A two-dimensional diode simulation setup is shown in Figure 3-8. The simulation is performed on a diode cross-section, where the light blue block in the center represents the intrinsic poly region with optical propogation going into and out of the page. The

p+ doped anode is on the left of the figure and the n+ doped cathode is on the right, with oxide on the top and bottom of the polysilicon sections. A fine mesh is defined around the polysilicon sections, and to decrease simulation time, a coarser mesh is used for the oxide regions.

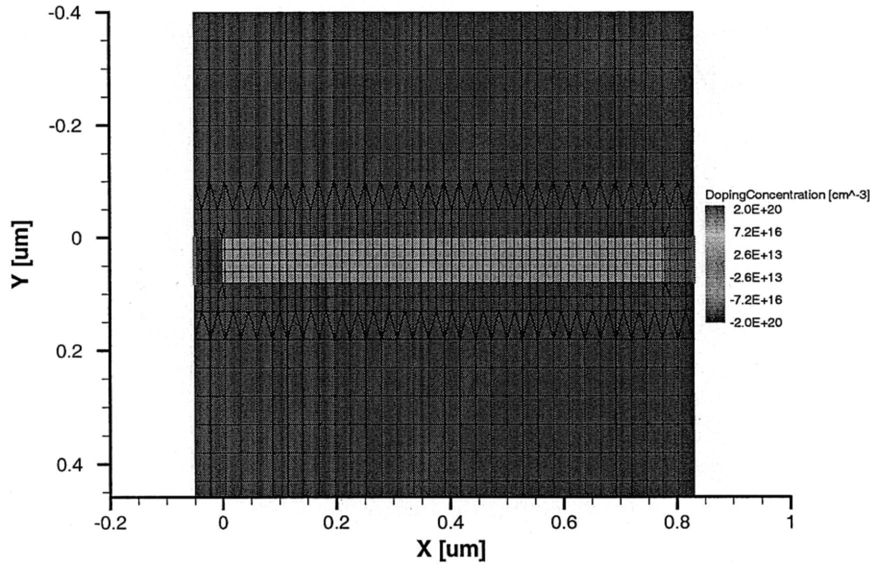


Figure 3-8: P-I-N cross-section showing Sentaurus simulation mesh.

This simple simulation setup allows several design tradeoffs to be analyzed. Poly thickness is set by the foundry and cannot be changed by the device designers, but the diode body (shown in Figure 3-8 across the x-axis) is one parameter that can be chosen. A small diode body length is good from an electrical perspective because it lowers the resistance of the device and increases the injected carrier density for a given voltage, as shown in the Sentaurus results in Figure 3-9 [4]. However, a diode body length smaller than the waveguide width will cause high through loss and will further decrease the overlap of the injected carriers with the optical mode.

The I-V curve of the diode is used at design time to determine some first-order qualities of the driver circuit, such as the on resistance and the required current

[4]Figure 3-9 shows data valid for silicon with a carrier lifetime of 1 μs. Polysilicon with a carrier lifetime of 1 ns achieves approximately 5x less carrier density at a bias of 1.0 V, but the shape of the graph (including the carrier concentration saturation) is similar

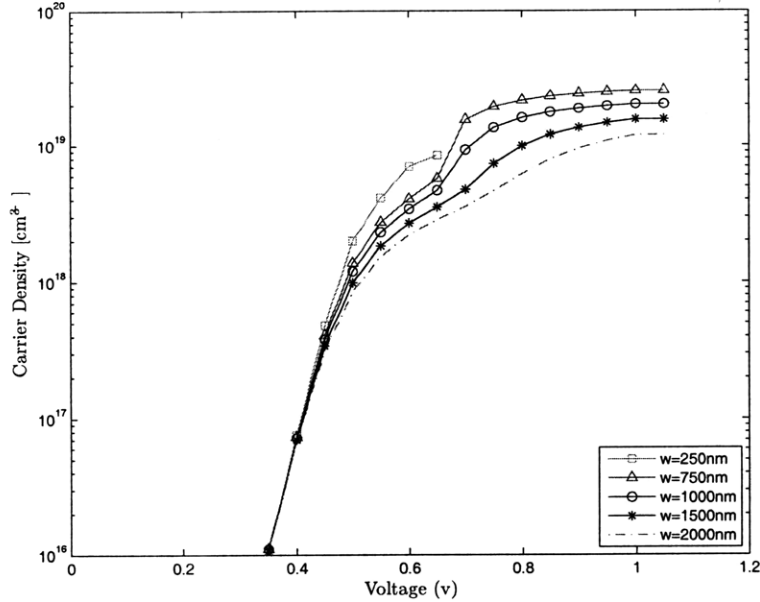


Figure 3-9: Simulated injected charge concentration vs. voltage.

drive necessary to reach a target voltage and charge concentration. The I-V curve is also dependent on the diode length. Figure 3-10 shows the simulated dependence on diode length. This simulation matches measured data from the 65 nm EOS1 chip in Figure 3-11 reasonably well for design purposes. The discrepancy in the graphs can be explained by several causes. The Sentaurus simulations do not model the series resistance of the interconnect to the diode. Also, the drawn diode length does not necessarily correspond to the fabricated length due to the dopant diffusion in the fingers.

3.4.2 Device Simulation using SPICE

The analysis of the previous section demonstrated a link between the injected charge in the I-region and the modulation depth. We modified a SPICE model of a power P-I-N diode under high injection [17] to represent the P-I-N modulator device [3]. This SPICE model implements a Padé approximation of the I-region charge using an RLC network. The total charge in the I-region is represented as a subcircuit node voltage, which is easily exported to MATLAB or other data processing tools. This

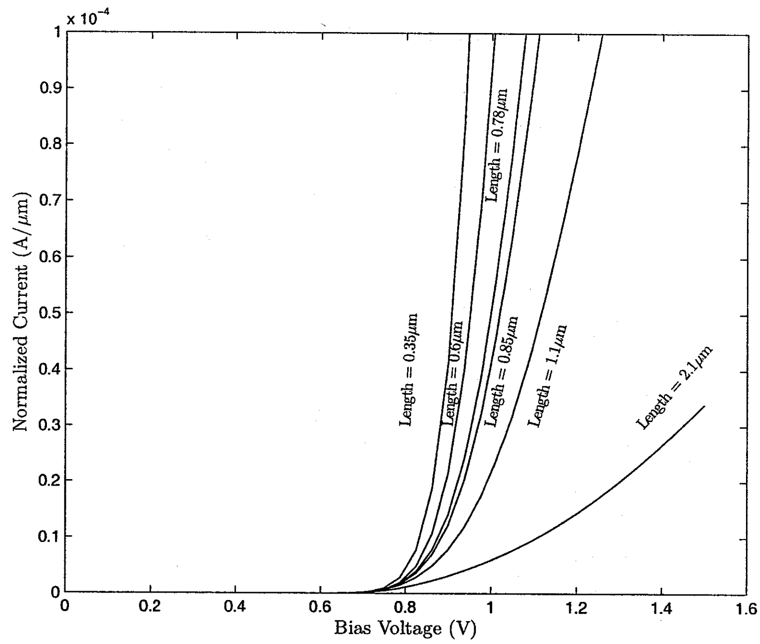


Figure 3-10: P-I-N I-V curve for various I-region lengths (Sentaurus).

SPICE model allows us to generate optical eye diagrams from electrical simulatons. This model is highly convenient for electrical simulations, but because its model is behavioral in nature, its accuracy is limited and needs to be calibrated with device simulations.

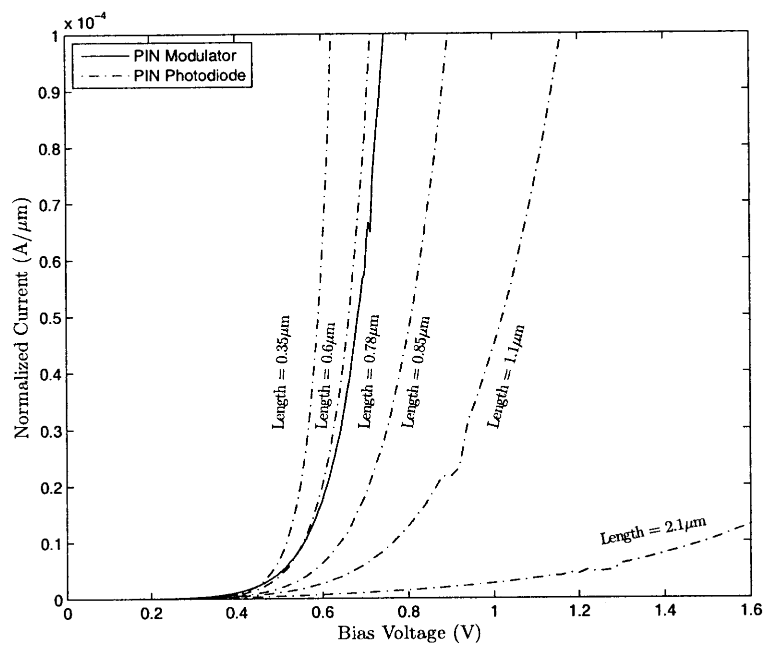


Figure 3-11: P-I-N I-V curve for various I-region lengths (EOS1 measured).

Chapter 4

The Modulator Driver

4.1 Introduction

The goal of the modulator driver is to inject charge into the P-I-N diode. This charge changes the index of refraction inside the I-region (the waveguide), blueshifting the ring modulator's resonant frequency and raising the transmissivity at the resonant frequency. In Chapter 3, both the ring modulator and its P-I-N diode were analyzed and Equation 3.53 provides a link between a target extinction ratio and the injected carrier concentration. This chapter describes the evolution of a modulator driver designed to inject the minimum amount of charge necessary to reach the target extinction ratio, resulting in high speed and high energy efficiency.

4.2 A Case for Pre-Emphasis

The first step in the development of the modulator driver is to analyze a simplified model to gain a basic understanding of the limits and requirements of the circuit. It is assumed that we have chosen a target extinction ratio (3 dB is a good choice) and that the analysis of Chapter 3 yielded a minimum $\Delta N_0 = 2.1 \times 10^{18}$ cm^{-3} necessary to reach that extinction ratio. The minimum injected charge necessary is $\Delta Q_0 = 1.9 \times 10^{-13}$ C.

The charge $Q(t)$ in the I-region follows a first-order linear differential equation,

where $i(t)$ is the diode current and τ_c is the carrier lifetime in the I-region [11].

$$\frac{dQ(t)}{dt} = i(t) - \frac{Q(t)}{\tau_c} \tag{4.1}$$

The solution to this equation makes the initial condition assumption that $Q(0) = 0$. Q_S is the steady-state charge in the I-region.

$$Q(t) = Q_S \left[1 - e^{-\frac{t}{\tau_c}}\right] \tag{4.2}$$

$$Q_S = \tau_c \cdot i(t) \tag{4.3}$$

The nonlinear relationship between the charge in the I-region and the optical transmissivity can be exploited to increase energy efficiency and speed. With a fixed driver resistance, on a transition from a 0 to a 1 bit, the charge in the I-region will steadily grow toward Q_S, reaching Q_S perhaps sometime in the middle of the bit. If the driver circuit provides $i(t)$ such that $Q_S = Q_0$, the resulting optical eye diagram will be poor at high speed due to the slow rising trajectory of $Q(t)$. A pre-emphasized driver can do much better. A driver with a much lower resistance for a small portion of the bit time on a 0 to 1 transition will increase the charge in the I-region much more rapidly, improving the optical eye diagram [20]. The total driver resistance during pre-emphasis is referred to as R_A, the resistance during the remaining forward bias portion of the bit time is R_B, and the reverse-bias driver resistance is R_C.

This pre-emphasis technique has three main advantages:

- It lowers the amount of steady-state charge necessary for a 1 bit, increasing energy effeciency.
- Because the amount of steady-state charge has been reduced, there is less chance of shifting all the way to the next optical channel.
- The modulator can operate at higher speeds.

To estimate the required driver resistance at a datarate of 5 Gb/s, it is assumed that the pre-emphasis driver will be active for the first quarter of a bit time for a 0 to 1 transition, or 50 ps. The goal of the pre-emphasis driver will be to raise $Q(t)$ to the level of Q_0 by the end of the pre-emphasis pulse. Although τ_c is unknown to at least an order of magnitude, a guess of 1 ns is not unreasonable.

$$Q(t = 50\,\text{ps}) = Q_0 = Q_{SA} \cdot (1 - e^{(-50\,\text{ps}/10\,\text{ns})}) \tag{4.4}$$

$$Q_{SA} = 3.9 \times 10^{-12}\,\text{C} \tag{4.5}$$

In a commercial CMOS process, V_{DD} is fixed, and is approximately 1.0 V at the 32 nm node. A digital driver circuit can be approximated to the first order by the circuit shown in Figure 4-1. R_{dr} is the total resistance of the driving transistors and R_S is the series resistance of the P-I-N diode. This simplification of the driver circuit is used to find an appropriate starting range for the driver resistance to make a first estimate at the transistor sizing.

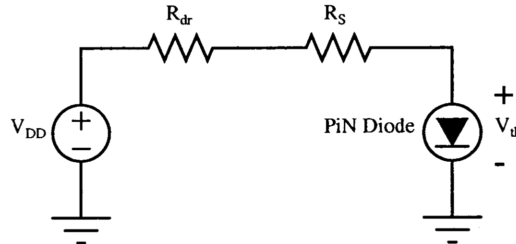


Figure 4-1: First order charge rise time schematic.

The high V_{th} of the P-I-N diode, shown earlier experimentally in Figure 3-11, means that a low R_S and R_{dr} are necessary to achieve a reasonable Q_S. The V_{th} of the modulator diode is approximately 0.8 V for currents in the range of 1 mA. The V_{DD} limit of the process is also a concern. For demonstrating short-term functionalality of the modulator driver, V_{DD} can be temporarily raised to 1.5 or 2.0 V if the driver cannot provide enough current at 1.0 V. This solution is not feasible for mainstream adoption of silicon photonics due to the degradated reliability of the circuits. It is

also important to note that above a certain bias voltage, the carrier concentration in the I-region begins to saturate, as shown in Figure 3-9, so increasing the voltage further may have little effect.

$$i(t) = \frac{V_{DD} - V_{th}}{R_A + R_S} \tag{4.6}$$

$$Q_{SA} = \tau_c \cdot \frac{V_{DD} - V_{th}}{R_A + R_S} \tag{4.7}$$

$$R_A + R_S = \tau_c \cdot \frac{V_{DD} - V_{th}}{Q_{SA}} = 51\Omega \tag{4.8}$$

With a diode contact resistance of approximately 30 Ω, the pre-emphasis driver resistance should be 20 Ω. Unfortunately, due to the high V_{th}, the transistors are likely to be in the triode region, and this target is difficult to achieve without an unreasonably large driver circuit.

Once the pre-emphasis pulse ends and the charge reaches the level of Q_0, the pre-emphasis driver will deactivate and the forward-bias driver will be active. The forward-bias driver will only sustain the charge at the level of Q_0.

$$R_B = \tau_c \cdot \frac{V_{DD} - V_{th}}{Q_0} - R_S = 1.0k\Omega \tag{4.9}$$

The forward-bias driver resistance is much more reasonable. We chose a nominal design point where the pre-emphasis driver is four times the strength of the forward-bias driver and two times the strength of the reverse-bias driver.

4.3 First Generation Modulator Driver

The first chip we fabricated, named EOS1, was intended primarily for characterizing and demonstrating different integrated optical structures. The chip was designed in a commercial 65 nm process and is the first integrated photonics chip to use bulk-CMOS. Its 2 mm x 2 mm^2 area is divided into horizontal test rows containing various

optical test structures, such as vertical grating couplers, paperclip loss measurement structures, waveguides of different widths, photodiodes, and modulators. A minimal number of Design Rule Check (DRC) waivers were necessary to tape out the design, proving that the technology is compatible with existing processes.

After the chip returns from the foundry it must be post-processed to remove the substrate directly underneath the waveguide to avoid high optical losses. Rows of etch vias extending from top-layer metal down to the substrate run laterally across the chip in close proximity to the waveguides. During postprocessing these vias are etched away, leaving holes from the top of the chip down to the substrate. Xenon difluoride gas is released into these holes, eating away the substrate underneath the etch row and the waveguide and leaving an air gap. The end result of this process is shown in Figure 4-2.

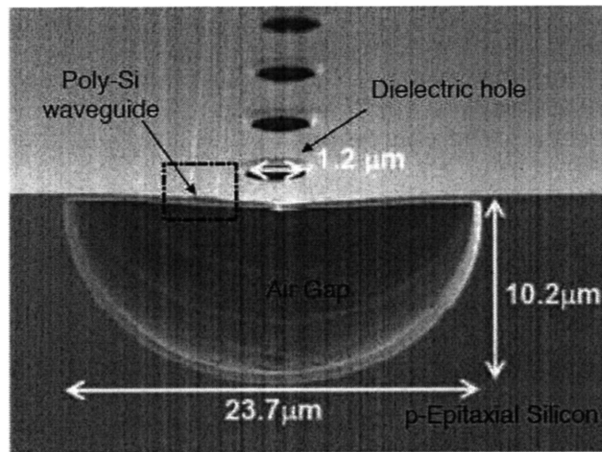


Figure 4-2: Cross section of an undercut waveguide.

The chip has eight standalone modulator drivers based on our best estimate of the diode properties. These eight modulators are the only electronics on the chip and is confined to the top row; the rest is dedicated solely to optical test structures.

The modulator driver is a custom digital push-pull circuit with sub-bittime pre-emphasis [20]. The schematic for the driver is shown in Figure 4-5 and the optical layout of the ring modulator is shown in Figure 4-4. A closer view of the electrical layout is shown in Figure 4-6.

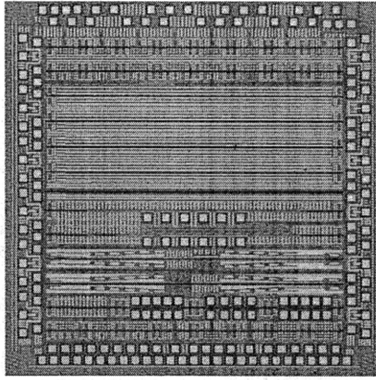


Figure 4-3: EOS1 die photo.

At the beginning of a zero to one transition, both the pre-emphasis driver and the forward-bias driver are active, maximizing the current into the I region. After a short time (less than a bit time), the pre-emphasis driver deactivates, lowering the current into the diode. The unbalanced weak driver has a strong NMOS and a weak PMOS. The strong NMOS ensures that there is a strong reverse bias for a one to zero transition, quickly sweeping the charge out of the I region. The pre-emphasis pulse only occurs during a zero to one transition. The modulator operates at 10 Gb/s in simulations.

The carrier lifetime of the poly-Si is unpredictable due to an unknown amount of defects and varies from fab to fab, so this parameter was difficult to estimate at the time of chip design. The operation of the modulator depends heavily on the carrier lifetime. To account for varying carrier lifetimes in the diode, two flavors of the modulator are included in the EOS1 chip. One flavor has a stronger weak driver than the other to adjust the charge injected into the diode. Experimental results are not yet available, but the energy efficiency is predicted to be approximately 50 fJ/bit. Once the post-processing of the chip is complete, measurements will be made to determine how well the SPICE model fits the characteristics of the modulator diode. DC measurements taken on the diode, shown in Figure 3-11 show a V_t dependence on the diode length, which is not included in the model. The diode's V_t is higher than was expected at design time, so the circuit must be run at higher than its target of 1.2 V.

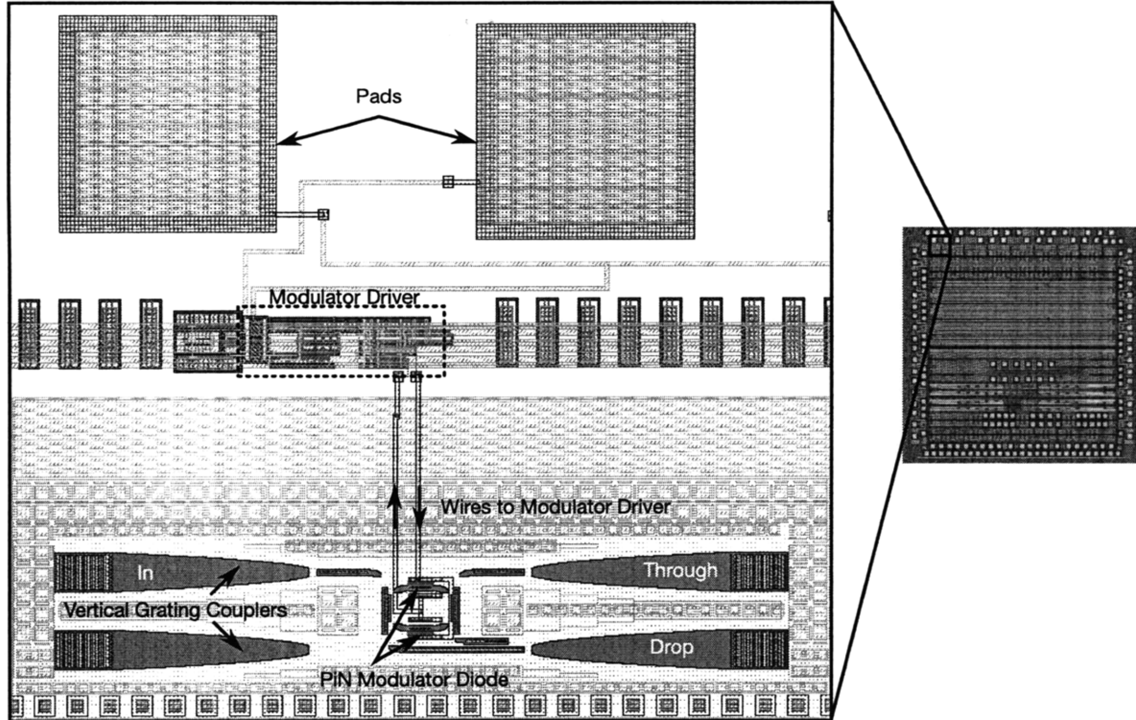


Figure 4-4: EOS1 modulator layout.

The unpredictable diode parameters such as carrier lifetime prompted a far more configurable design for the next chip to account for process uncertainty. The lack of electrical output in the EOS1 design made lab testing and debugging particularly tricky, which led us to develop more sophisticated infrastructure for the next chip.

4.4 Second Generation Modulator Driver

Although testing of the 65 nm chip was not complete, we had an opportunity to fabricate a second chip, EOS2, using a state-of-the-art TI 32 nm bulk-CMOS process. The goal of this second chip is to create an entire on-chip optical link.

The second generation modulator driver, shown below in Figure 4-7, is another custom digital push-pull circuit with sub-bittime preemphasis. The P-I-N diode is either forward or reverse biased by the three sets of pull-up and pull-down elements, and the strength of these elements can be digitally tuned across four bits.

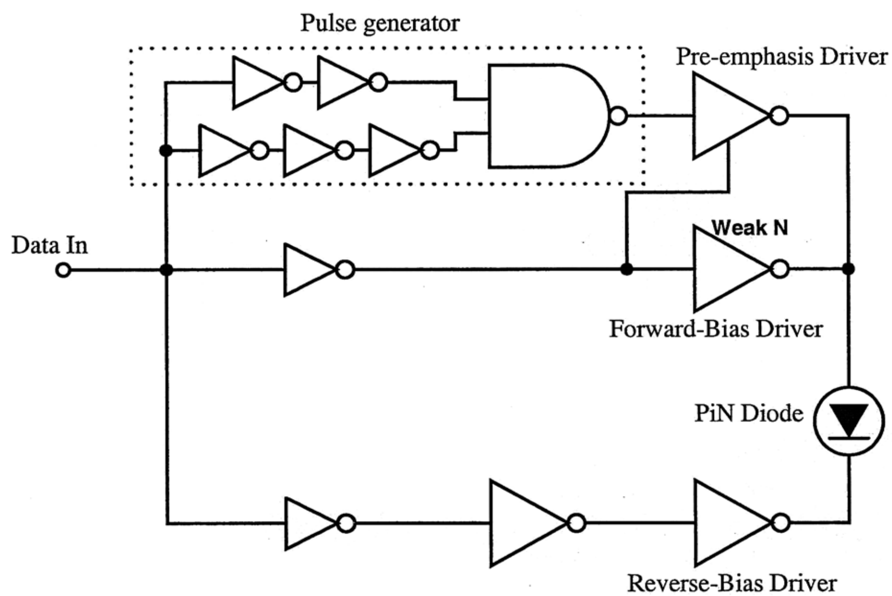


Figure 4-5: First generation (EOS1) modulator driver schematic

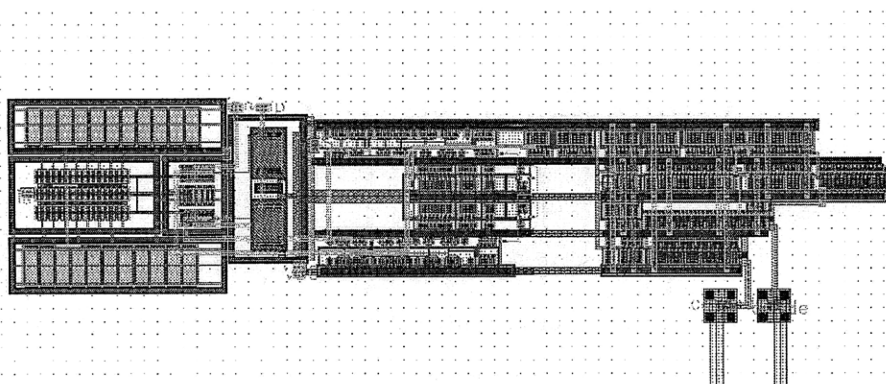
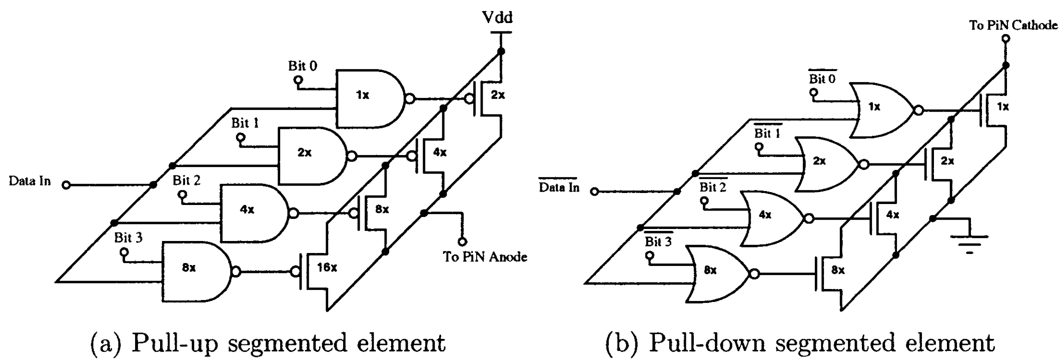


Figure 4-6: EOS1 CML to CMOS converter and modulator driver layout

Figure 4-7: Schematic of second-generation (EOS2) modulator driver.



(a) Pull-up segmented element

(b) Pull-down segmented element

Figure 4-8: Pull-up and pull-down elements.

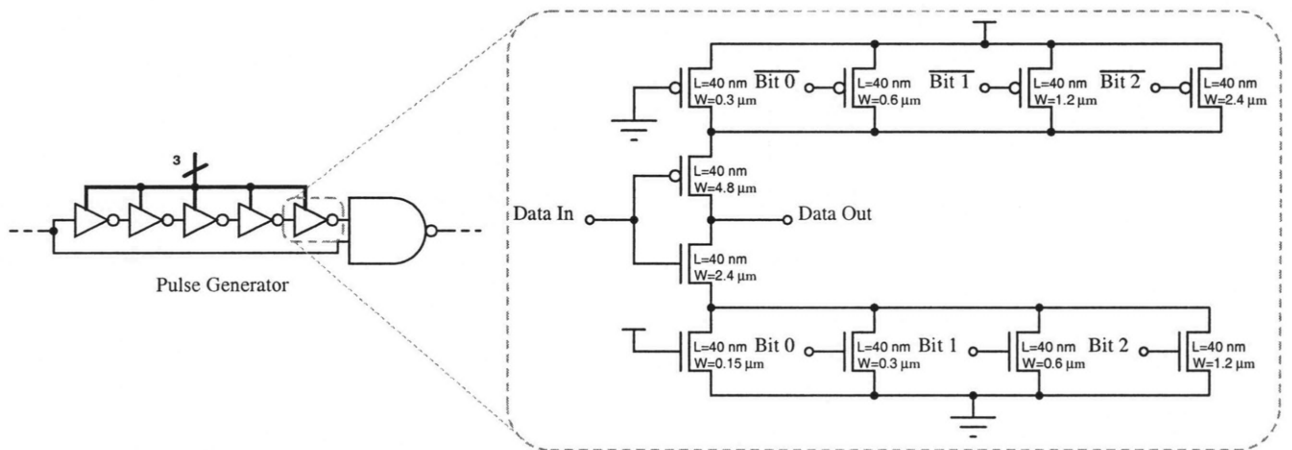


Figure 4-9: Conceptual schematic of second-generation (EOS2) modulator driver.

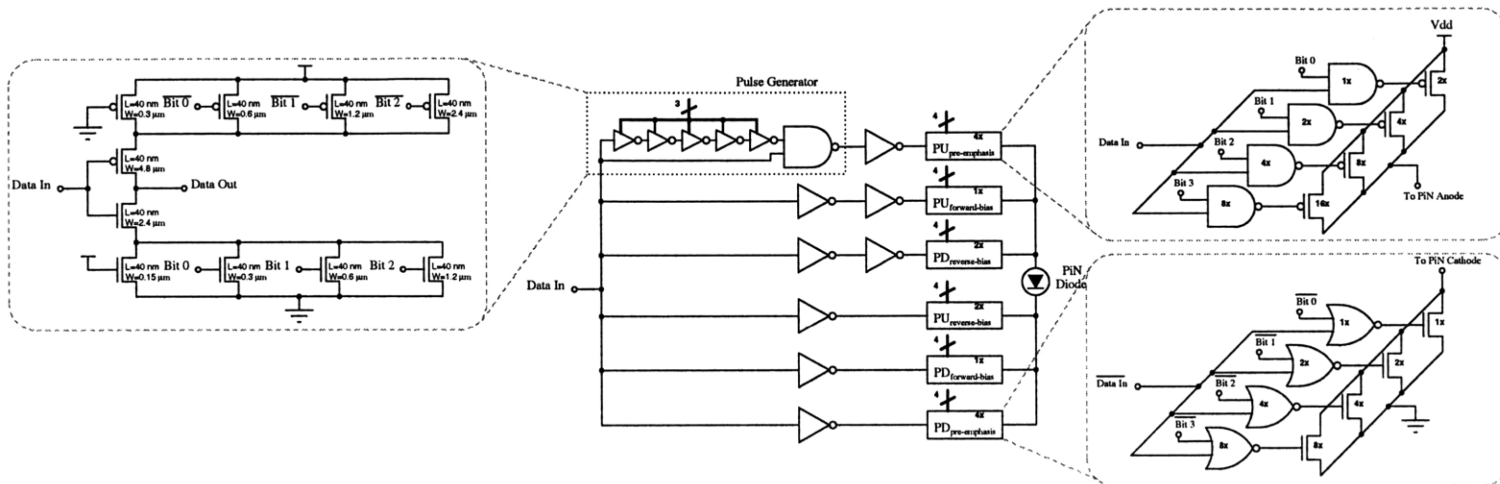
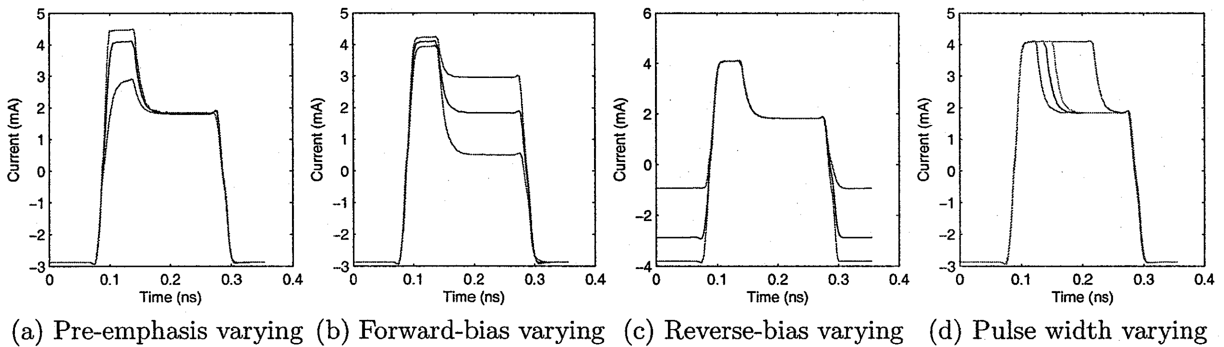


Figure 4-10: Conceptual schematic of second-generation (EOS2) modulator driver.

The four configurable elements of the pre-emphasis profile are seen in Figure 4-11. The wide range of configurability will be able to adapt to the uncertain device properties of the P-I-N diode. If the models for the diode are reasonably accurate, then the modulator should work at its designed speed of 5 Gb/s (see Figure 4-12). If the carrier lifetime is between 100 ps and 1 ns, simulations suggest the modulator can also work at 10 Gb/s. The driver currents for pre-emphasis, forward bias, and reverse bias can be tuned to within an order of magnitude. The duration of the pre-emphasis pulse can be tuned in the range of 10 ps to 100 ps.



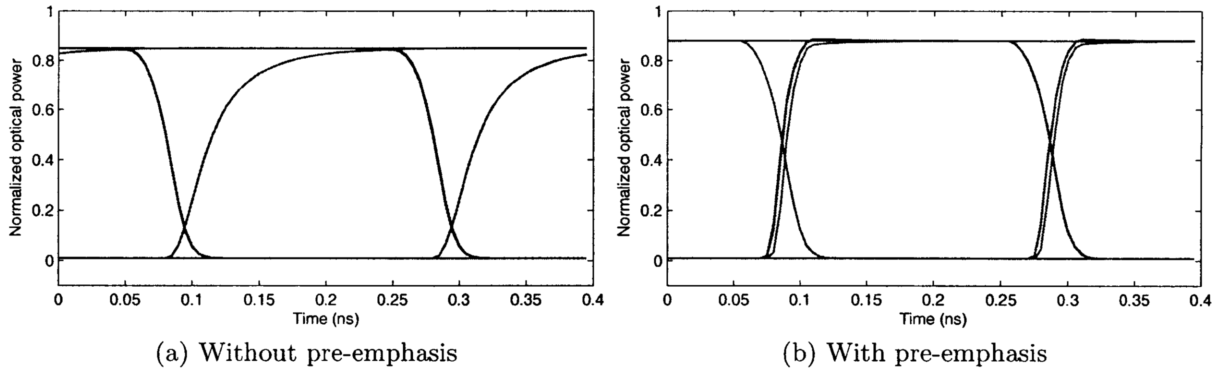
(a) Pre-emphasis varying (b) Forward-bias varying (c) Reverse-bias varying (d) Pulse width varying

Figure 4-11: Configurable parameters of the P-I-N current profile.

A major limitation of the previous EOS1 chip is that the modulators are standalone elements that must be individually tested by looking at the optical output. If the vertical couplers perform poorly, it is difficult to determine if the modulator is working correctly or not. The EOS2 chip is electrically far more sophisticated - in addition to modulators, this chip also has configurable data receivers, configurable clock receivers, and data snapshot buffers. A serial scan chain allows the bits to be set and read easily by an FPGA or a similar external circuit. The scan chain architecture makes it much easier to test and debug the EOS2 chip.

4.5 Conclusion

The previous chapter showed the link between optics and circuits by analytically determining the charge injection necessary to achieve a target extinction ratio. This



(a) Without pre-emphasis

(b) With pre-emphasis

Figure 4-12: 5 Gb/s eye diagram, 1 ns carrier lifetime (random data)

chapter showed the development of a driver circuit designed to inject that amount of charge quickly into the P-I-N diode structure by using pre-emphasis to take advantage of the nonlinear optical transfer function.

Chapter 5

Conclusion

As multi-core systems become more prevalent, new technologies will be needed to solve the bandwidth problem. Silicon photonics is a budding technology with the potential to have a large impact on the computing market if it can be economically integrated with current CMOS processes. While previous efforts in the field have relied on esoteric processing techniques such as thick-oxide SOI, our group has developed a method to enable silicon photonics in commercial bulk CMOS. We have taped out two test chips to demonstrate the feasibility of this new method.

Several building blocks are necessary to create a working integrated optical link. The focus of this thesis is on the modulator design as one of those primary building blocks, the modulator. The ring modulator was analyzed simultaneously from the device, circuit, and architecture perspectives, and the experiments with the two test chips are ongoing.

Appendix A

Tables

Component	Preliminary Design	Power Loss	Optimized Design	Power Loss
Coupler loss	1 dB/coupler	3 dB	1 dB/coupler	3dB
Splitter loss	0.2 dB/split	1 dB	0.2 dB/split	1dB
Non-linearity	1 dB	1 dB	1 dB	1 dB
Through loss	0.01 dB/ring	3.17 dB	0.01 dB/ring	3.17 dB
Modulator insertion loss	1dB	1dB	0.5 dB	0.5 dB
Crossing loss	0.2 dB/crossing	**12.8 dB**	0.05 dB/crossing	**3.2 dB**
On-chip waveguide loss	5 dB/cm	**20 dB**	1 dB/cm	**4 dB**
Off-chip waveguide loss	0.5×10^{-5} dB/cm	0 dB	0.5×10^{-5} dB/cm	0 dB
Drop loss	2.5 dB/drop	**5 dB**	1.5 dB/drop	**3 dB**
Photodetector loss	0.1 dB	0.1 dB	0.1 dB	0.1 dB
Receiver sensitivity	-20 dBm	-20 dBm	-20 dBm	-20 dBm
Power per wavelength		26.07 dBm		-1.03 dBm
		(0.40 W)		(0.78 mW)
Power required at source		***3.3 kW***		***6.38 W***

Table A.1: Optical Power Budget

Component	Latency
Serializer/Deserializer (50 ps each)	50 ps
Modulator driver latency	108 ps
Through latency (2.5 ps/adjacent channel)	7.5 ps
Drop latency (20 ps/drop)	60 ps
Waveguide latency (106.7 ps/cm)	427 ps
SM fiber latency (48.3 ps/cm)	483 ps
Photodetector + TIA latency	200 ps
Total latency	**1.385 ns**

Table A.2: Optical Data Transmission Latency

Symbol	Description and Nominal Units
L_j	Length of single diode junction in direction of optical propagation [m]
H	Waveguide height, determined by thickness of polysilicon layer [m]
W	Waveguide width transverse to the direction of optical propogation [m]
r	Ring radius in curved section of racetrack [m]
L_{tot}	Total circumference of ring resonator [m]
V_j	Single waveguide diode junction volume [m^3]
V_{tot}	Total ring modulator volume including waveguide and I-region volumes [m^3]
x	Position variable along diode length transverse to direction of optical propogation
L_d	Diode length (similar to waveguide width W)
W_d	Diode width (equivalent to junction length L_j
c	Speed of light in free space; 3×10^8 m/s
c_0	Speed of light in waveguide prior to index shift [m/s]
q	Electron charge; 1.602×10^{-19} C
ϵ_0	Permittivity of free space; 8.854×10^{-12} F/m
$m_{ce}*$	Conductivity effective mass of electrons [kg]
$m_{ch}*$	Conductivity effective mass of holes [kg]
λ_0	Wavelength of ring resonance at target optical channel [m]
λ_i	Wavelength of ring resonance after charge injection [m]
k_0	Wavenumber of light at ring resonance [m^{-1}]
k_i	Wavenumber of light after charge injection [m^{-1}]
ω_0	Angular frequency of ring resonance [rad/s]

f_0	Frequency of ring resonance [Hz]
FSR	Ring resonator free spectral range [Hz]
k_{FSR}	Wavenumber of free spectral range [m^{-1}]
ω_{FSR}	Angular frequency of free spectral range [rad/s]
$\mathbb{Q}$	Quality factor of ring resonator
m	Non-zero integer number of wavelengths in a round trip around the ring at resonance
Δm	Pertubation to m due to charge injection
Δk	Pertubation to k_0 due to charge injection
T_0	Transmissivity of ring filter at λ_0 prior to charge injection
T_{0dB}	Transmissivity of ring filter at λ_0 prior to charge injection [dB]
T	Transmissivity of ring filter at λ_0 after charge injection
T_{dB}	Transmissivity of ring filter at λ_0 after charge injection [dB]
h	Extinction ratio at λ_0
h_{dB}	Extinction ratio at λ_0
Δf	Frequency shift of ring resonance due to charge injection [Hz]
$\Delta\phi_{HWHM}$	Half-width-half-maximum phase shift to light at λ_0 due to charge injection
$\Delta\phi_{FWHM}$	Full-width-half-maximum phase shift to light at λ_0 due to charge injection
Δf_{HWHM}	Half-width-half-maximum resonant frequency shift due to charge injection [Hz]
Δf_{FWHM}	Full-width-half-maximum resonant frequency shift due to charge injection [Hz]
$\overline{E_0}$	$\overline{E}$-field vector representing light in the waveguide prior to charge injection [V/m]
$\overline{E_i}$	$\overline{E}$-field vector representing light in the waveguide after charge injection [V/m]
$\underline{E_0}$	Complex phasor representing $\overline{E}$-field magnitude at λ_0 [V]
n	Refractive index in unperturbed polysilicon
n_g	Group index of ring waveguide
Δn	Change in refractive index due to carrier injection (or temperature change)
Δn_e	Change in refractive index due to injected electrons
Δn_h	Change in refractive index due to injected holes
Δn_{eff}	Effective index change due to charge injection
Γ	Waveguide mode overlap coefficient
n_{fe}	Polysilicon free electron index change coefficient [cm^{-3}]
n_{fh}	Polysilicon free electron index change coefficient [cm^{-3}]
ΔN	Injected electron-hole pair concentration in the diode I-region [cm^{-3}]
ΔN_e	Injected electron concentration injected in the diode I-region [cm^{-3}]
ΔN_h	Injected hole concentration in the diode I-region [cm^{-3}]

Symbol	Description
ΔN_0	Required injected free carrier concentration to achieve a 3 dB extinction ratio [cm^{-3}]
ΔN_{tot}	Required number of injected free carriers to achieve a 3 dB extinction ratio
ΔQ_0	Required amount of injected charge to achieve a 3 dB extinction ratio
γ	Injection ratio
$\Delta\phi'$	Phase change to light at λ_0 from a single P-I-N diode junction due to charge injection
$\Delta\phi$	Phase change to light at λ_0 from both diode junctions due to charge injection
t	Time [s]
$Q(t)$	Total injected charge in I-region [C]
Q_S	Steady-state charge in I-region [C]
τ_c	Polysilicon carrier lifetime [s]
$i(t)$	Diode current [A]
V_D	Diode bias voltage [V]
V_{DD}	Supply voltage [V]
V_{th}	Diode threshold [V]
R_{dr}	Effective driver resistance
R_A	Effective pre-emphasis driver resistance
R_B	Effective forward-bias driver resistance
R_C	Effective reverse-bias driver resistance
R_S	P-I-N diode series contact resistance

Table A.3: Symbol description

Appendix B

Figures

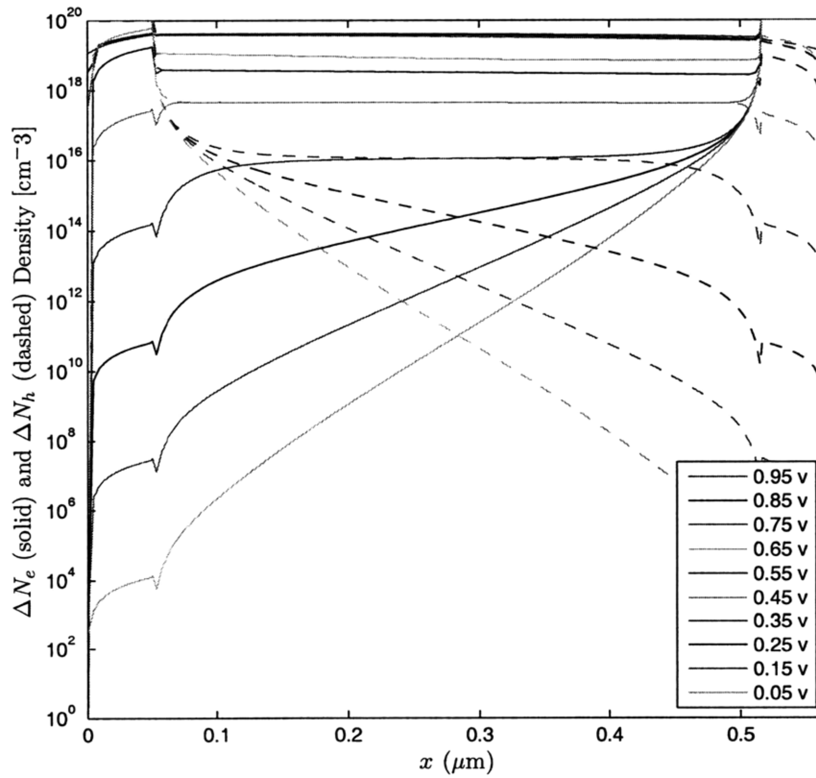


Figure B-1: Free electron and hole concentrations

Figure B-1 shows equal ΔN_e and ΔN_h above $V \approx 0.4\,\text{V}$ in a forward-biased P-I-N diode (from Sentaurus simulations). The I-region extends from $x = 0.05\,\mu\text{m}$ to $x = 0.515\,\mu\text{m}$.

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